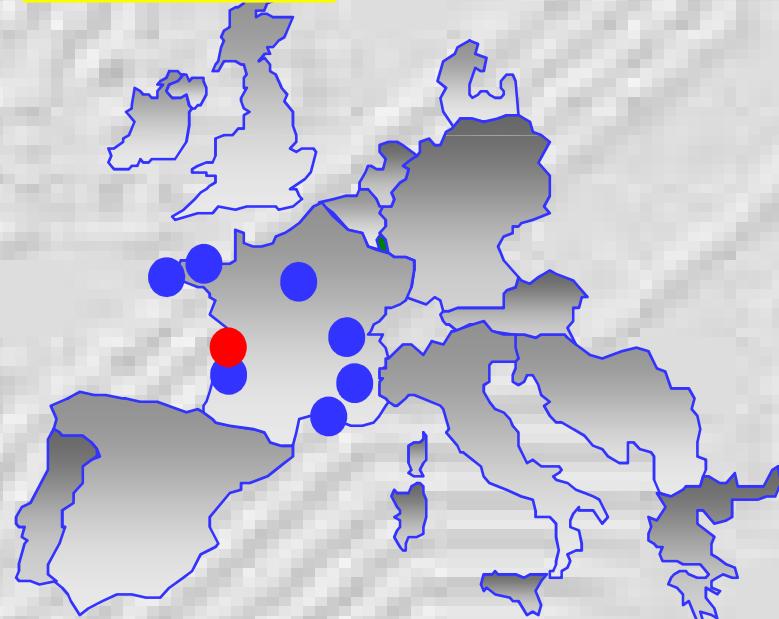
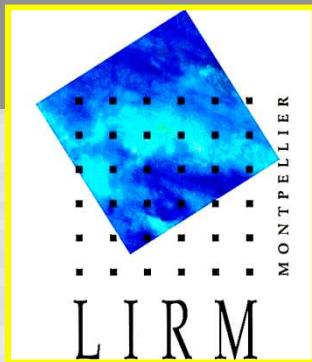
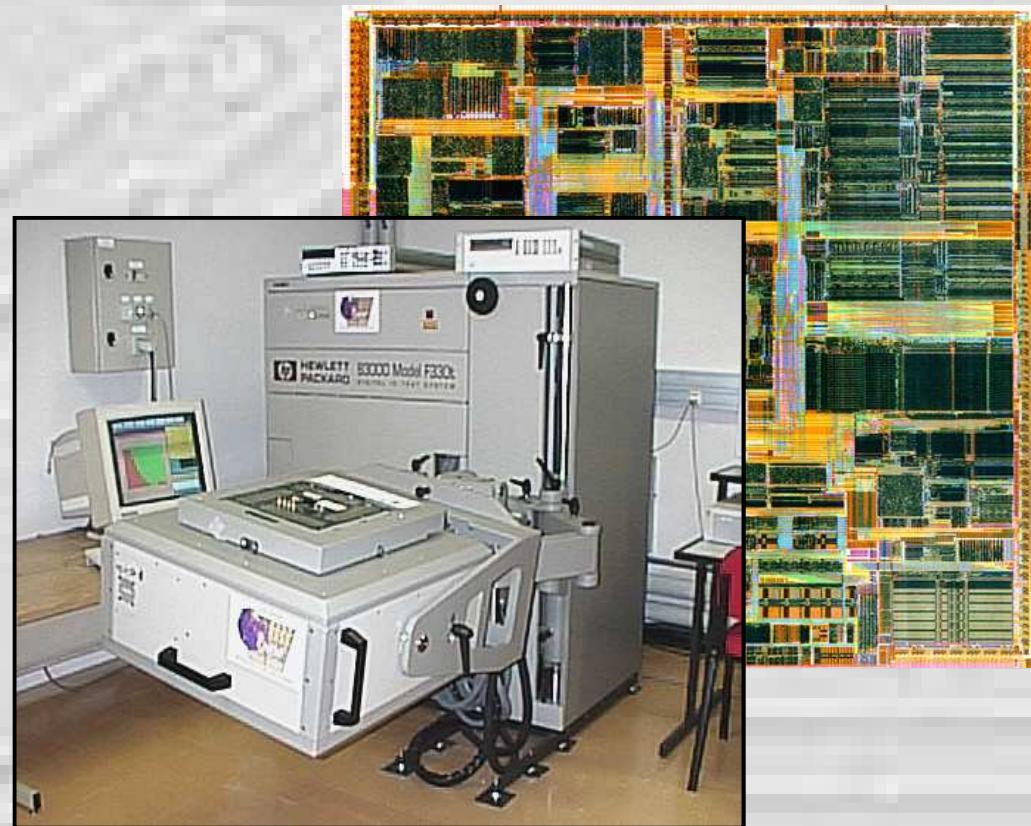


Fundamentals of Digital & Analog System Testing



Michel Renovell



Ecole Numérique IN2P3

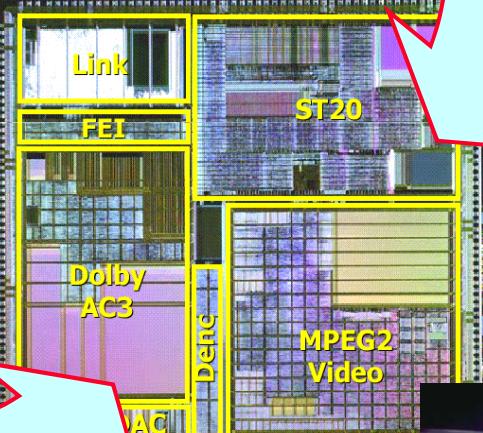
Introduction

IN2P3



Application

```
process begin  
  wait until not  
    CLOCK'stable  
    and CL  
  if(ENABLE  
    TOGGLE;  
  end if;  
end process
```



Test (preparation)



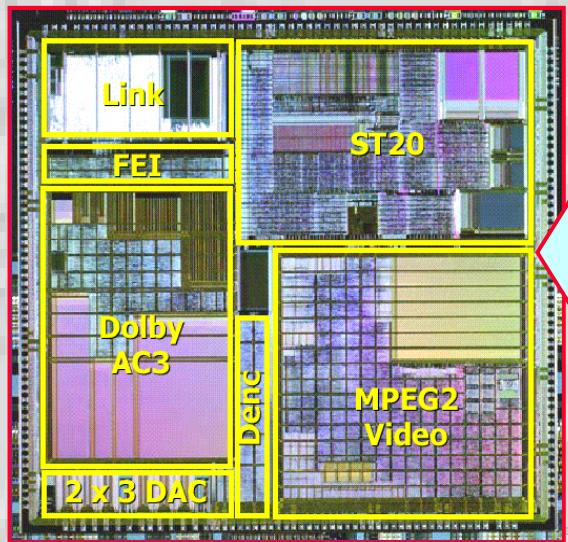
Technology

Design

Test

Introduction

Design Error



Design

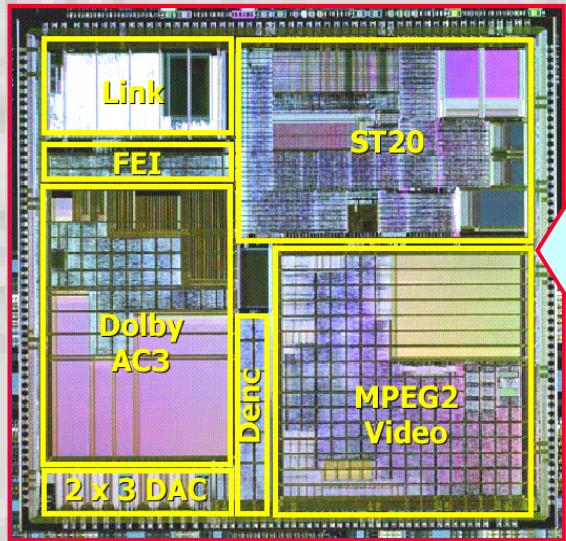
Layout

Manufacturing

Deviation & Spot



Introduction



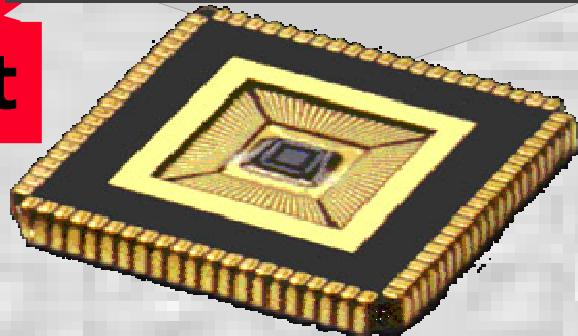
```
process begin  
wait until not  
CLOCK'stable  
and CLOCK=1;  
if(ENABLE='1') then  
TOGGLE<= not  
TOGGLE;  
end if;  
end process;
```

Design

Layout

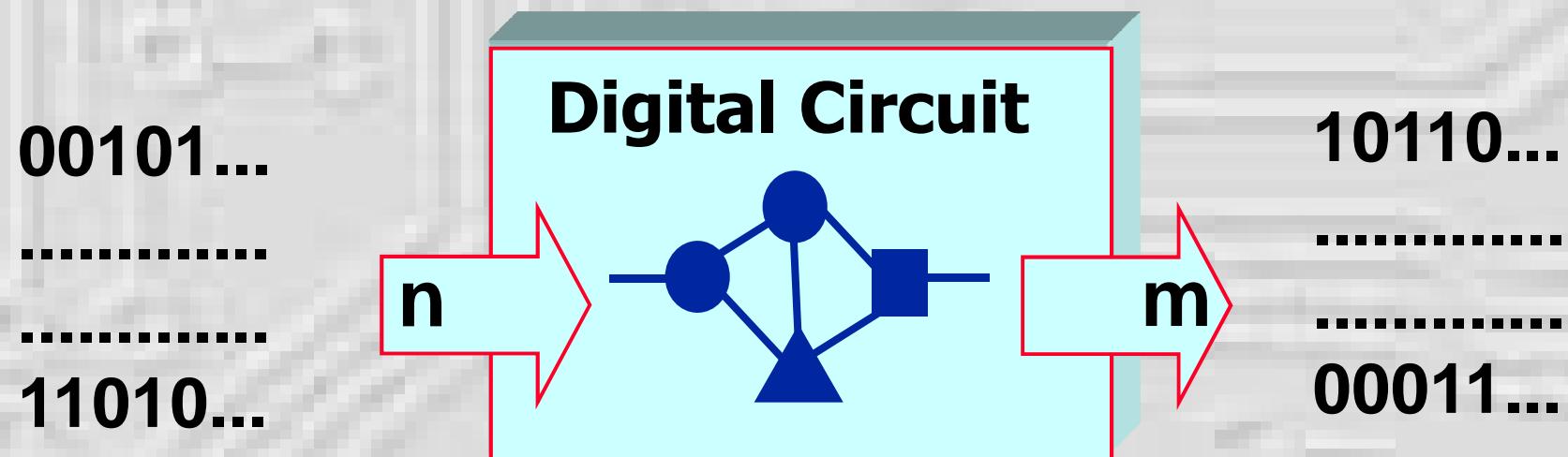
Manufacturing

Deviation & Spot



Introduction

IN2P3

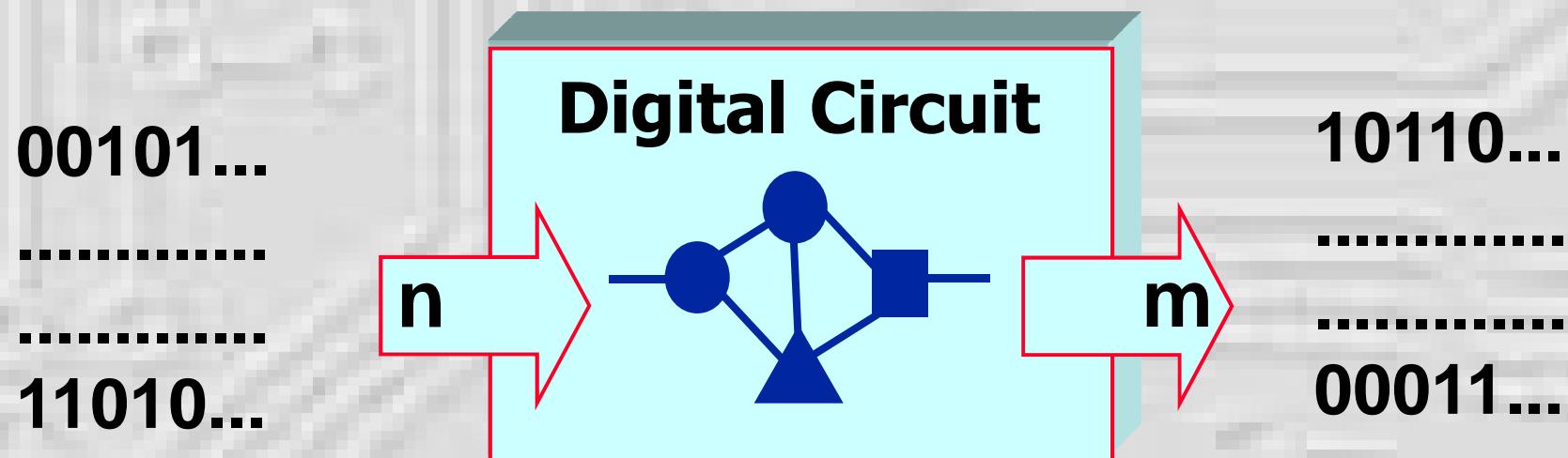


- Boolean Testing
- Test Patterns
- Go/NoGo



Introduction

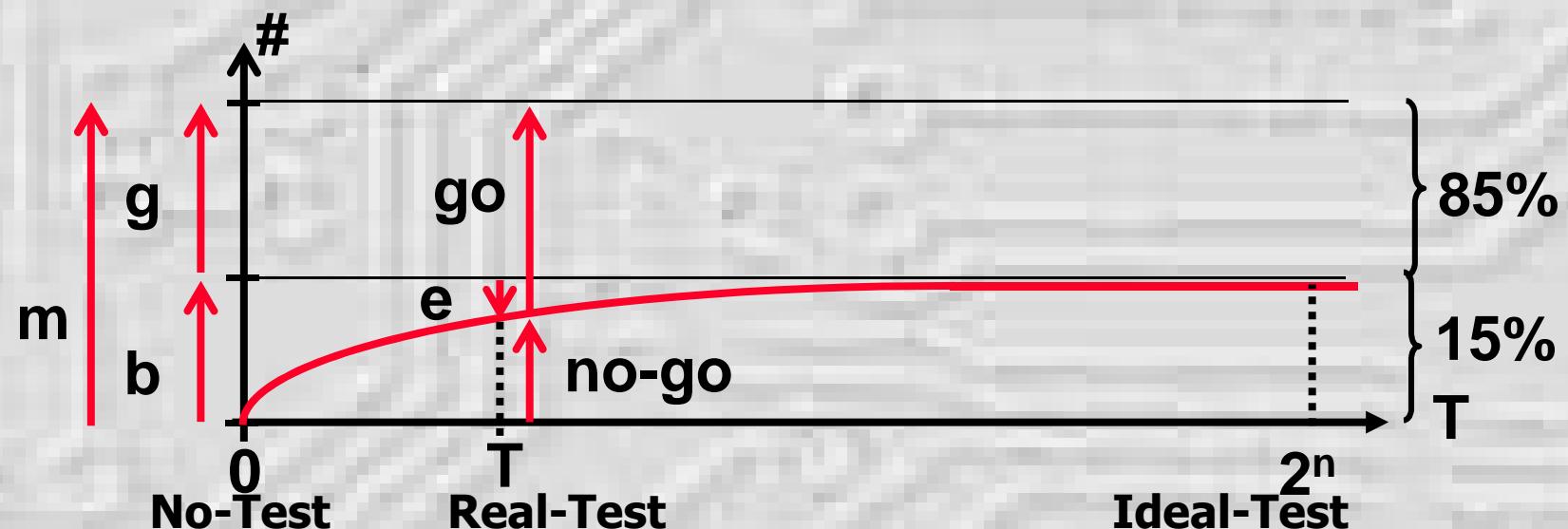
IN2P3



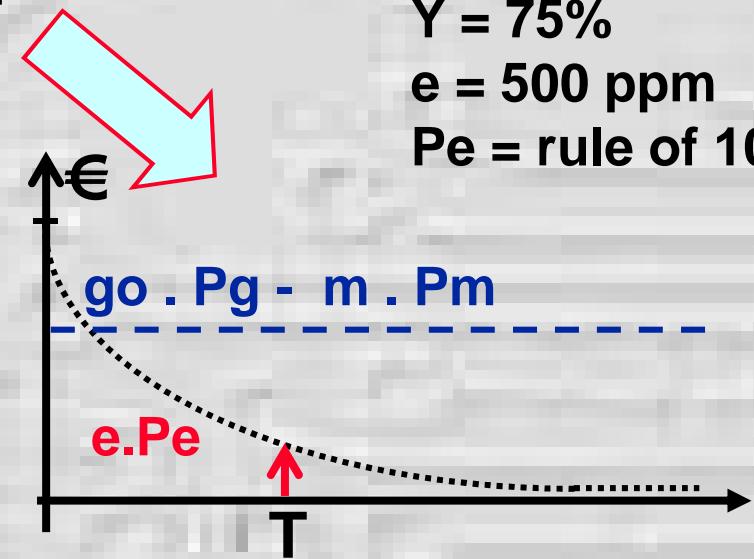
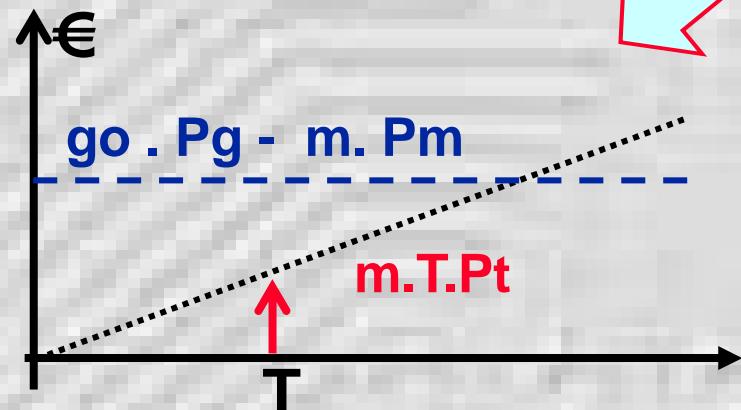
- Exhaustive Testing
- 2^{64} patterns
- $10^{20}/100\text{MHz} = 10^{12}\text{s}$
- => 5850 years

- Realistic Test
- 10s / 100MHz
- 10^9
- $1 / 10^{11}$

Introduction

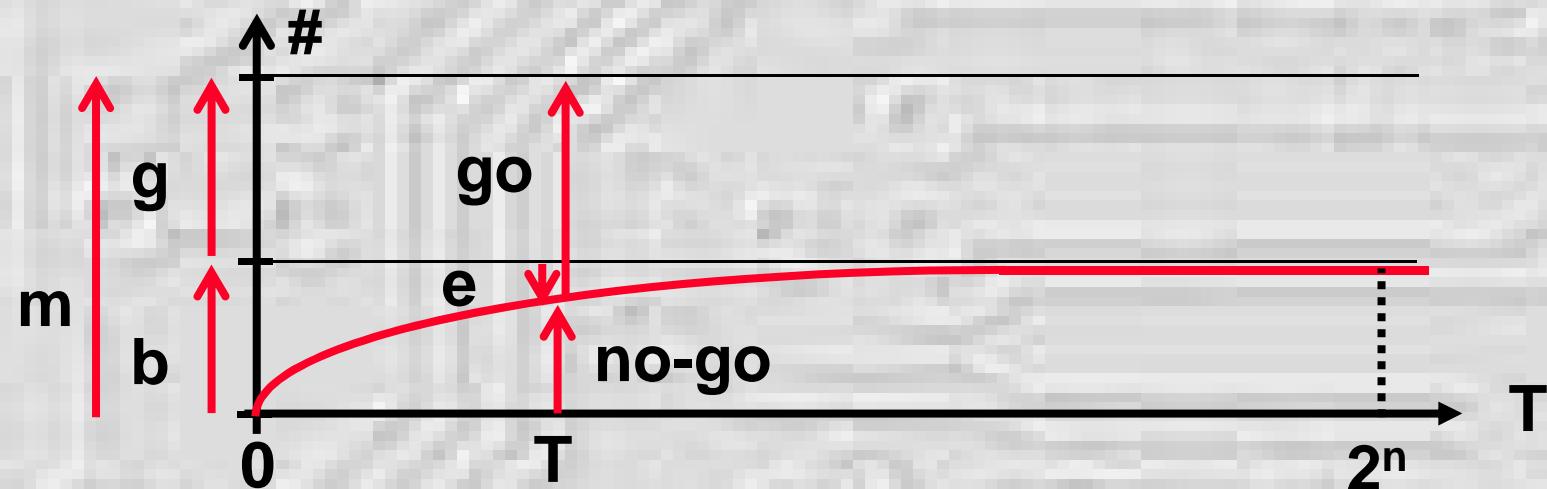


$$go \cdot Pg - m \cdot Pm > \text{Margin}$$

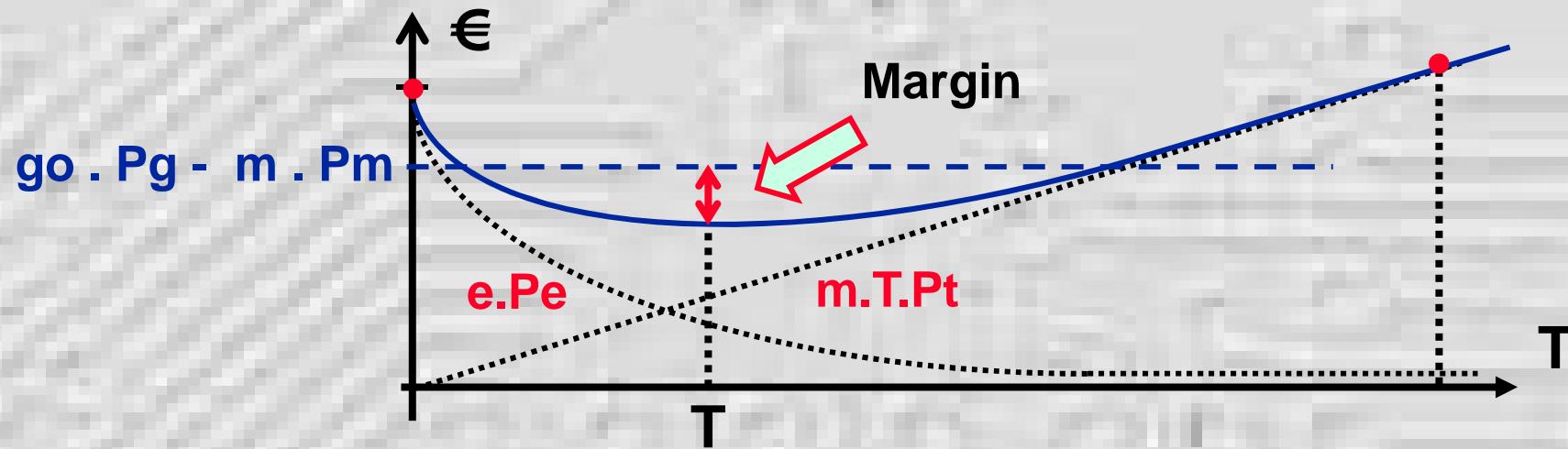


$Y = 75\%$
 $e = 500 \text{ ppm}$
 $Pe = \text{rule of 10}$

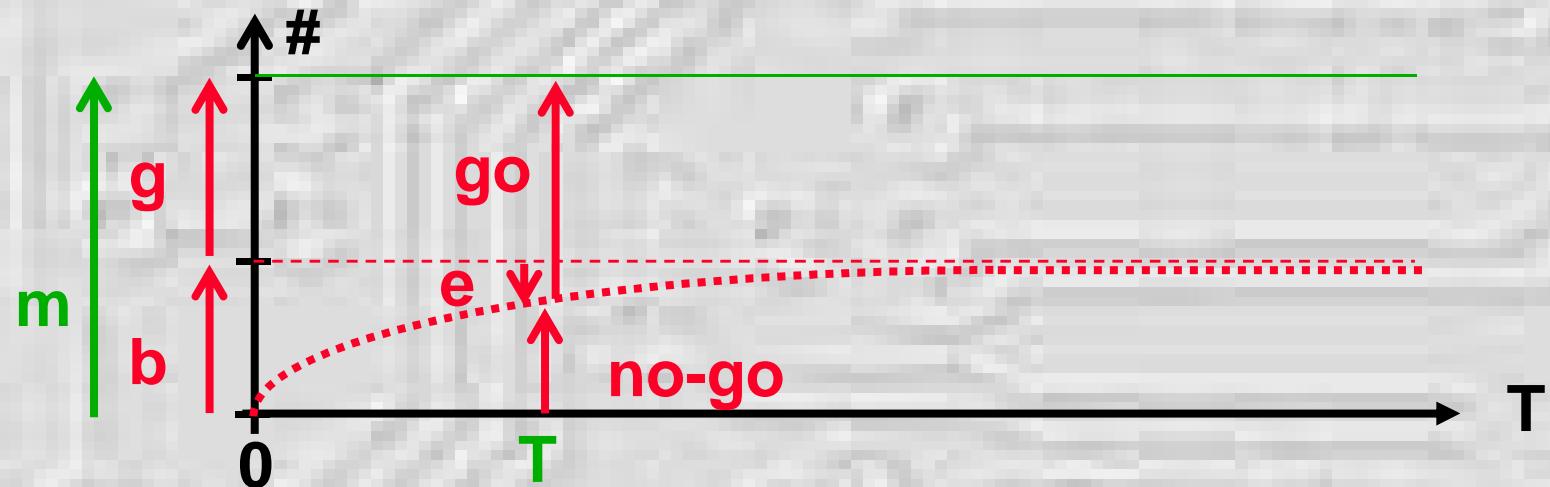
Introduction



$$go \cdot Pg - m \cdot Pm \geq m \cdot T \cdot Pt + e \cdot Pe$$

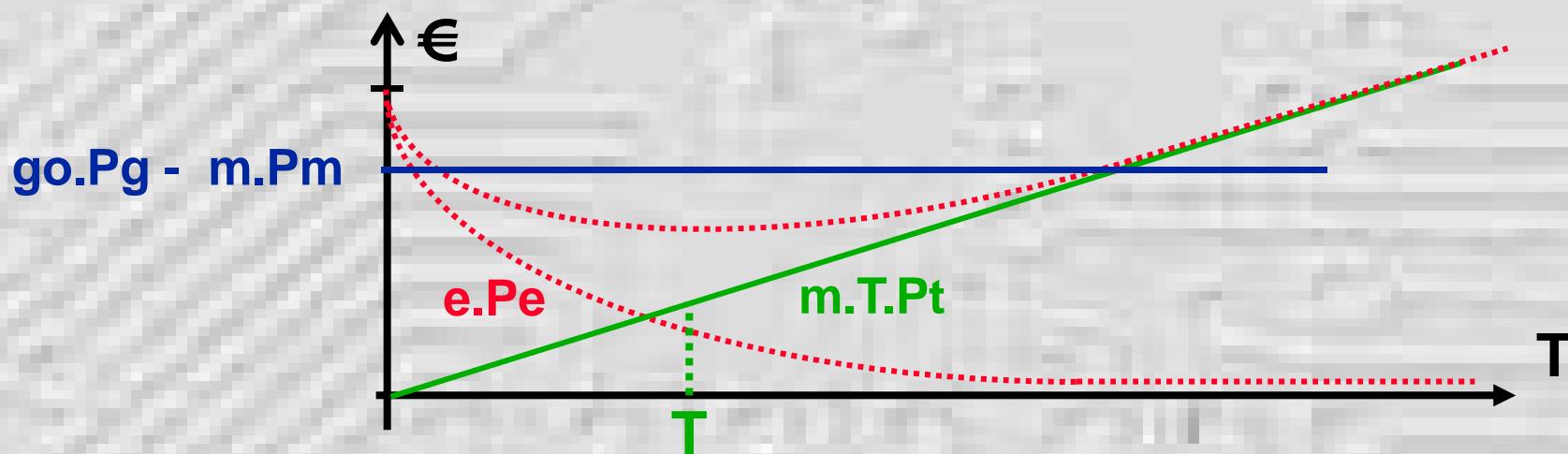


Introduction

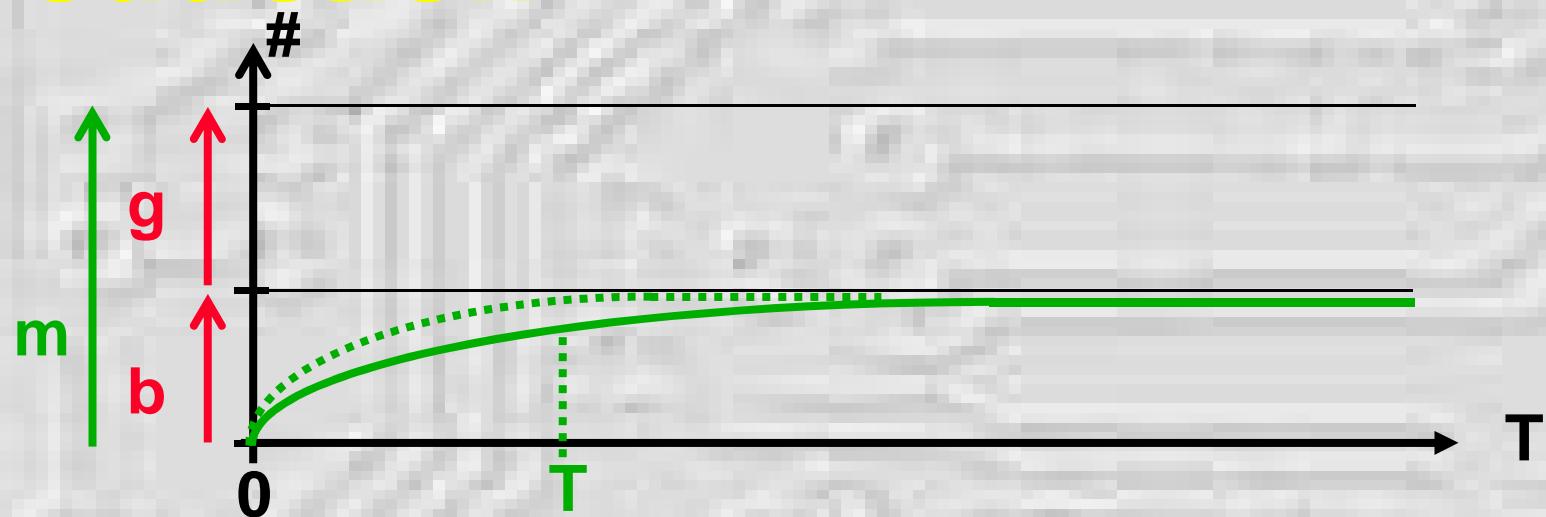


I) Criteria to stop the test generation

=> Estimate how many faulty circuits not yet detected (e?)

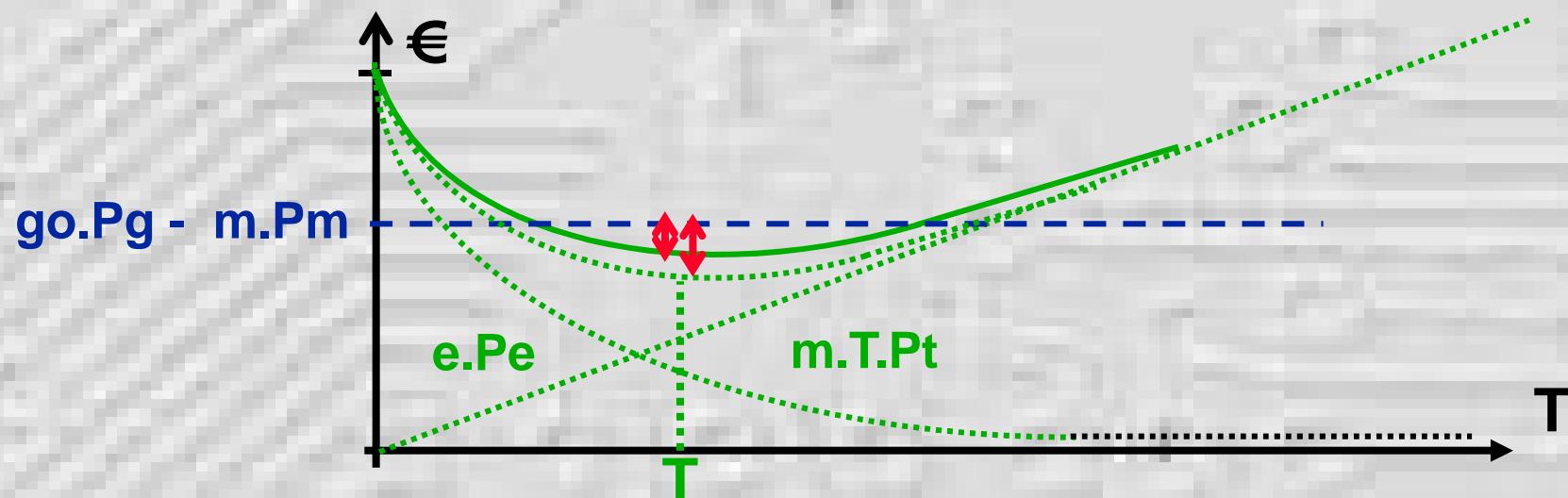


Introduction

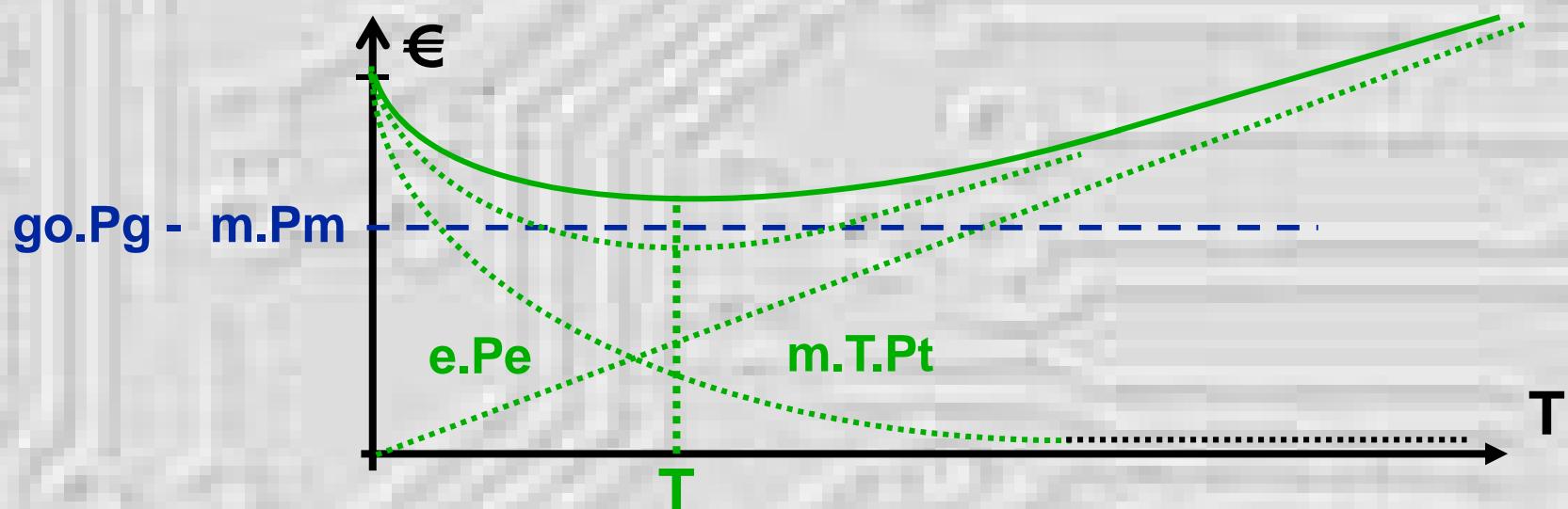


II) Criteria to optimize the test generation

=> Estimate how many faulty circuits are detected by each vector

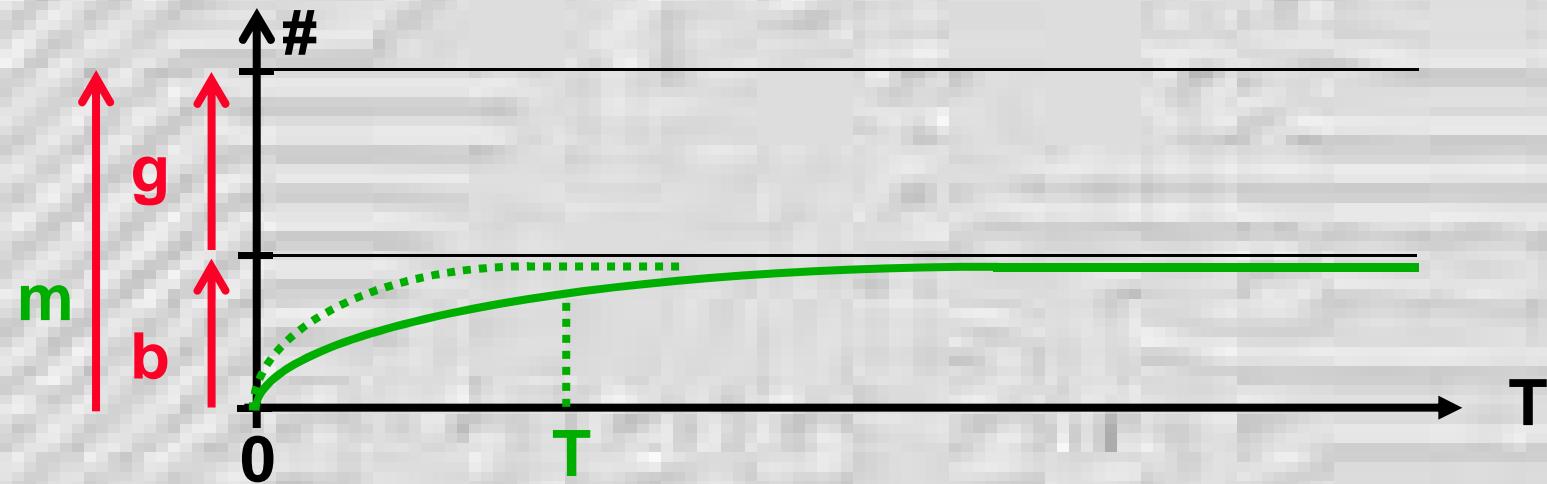


Introduction



III) Criteria to make circuit Testable

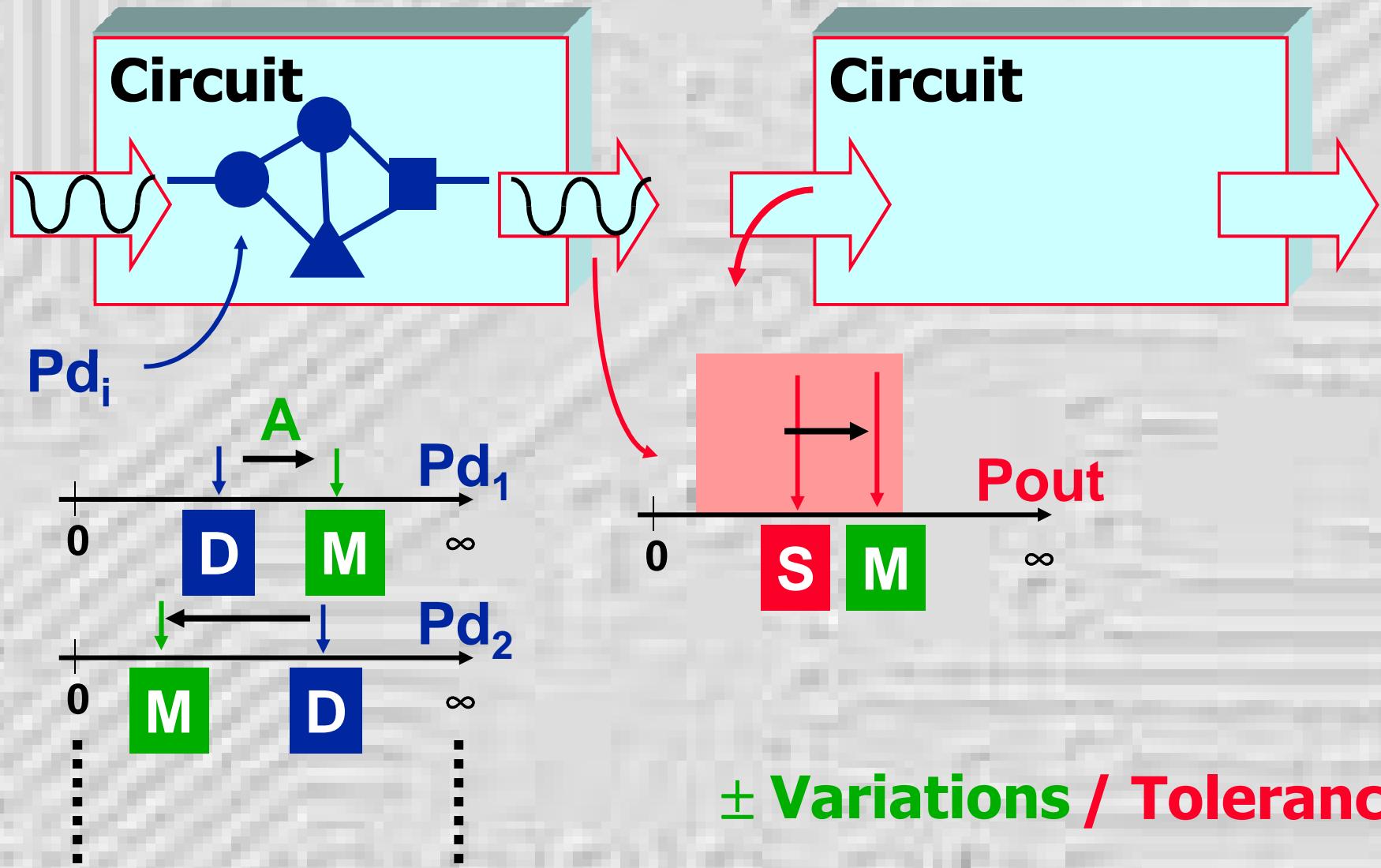
=> Propose circuit modifications



Fundamental Properties

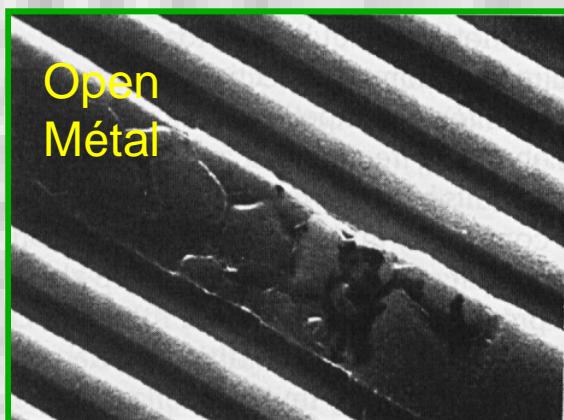
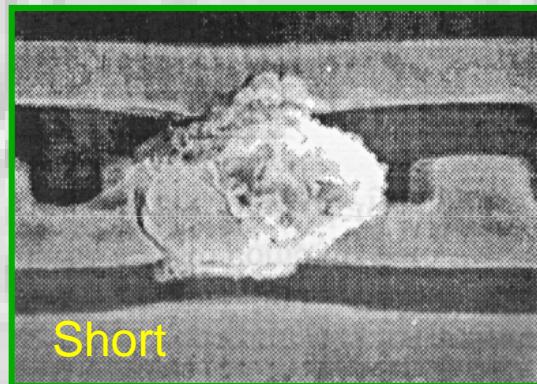
Fund. Props

IN2P3

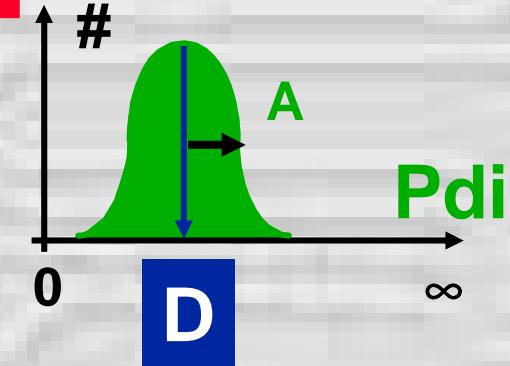


Fund. Props

± Variations ?

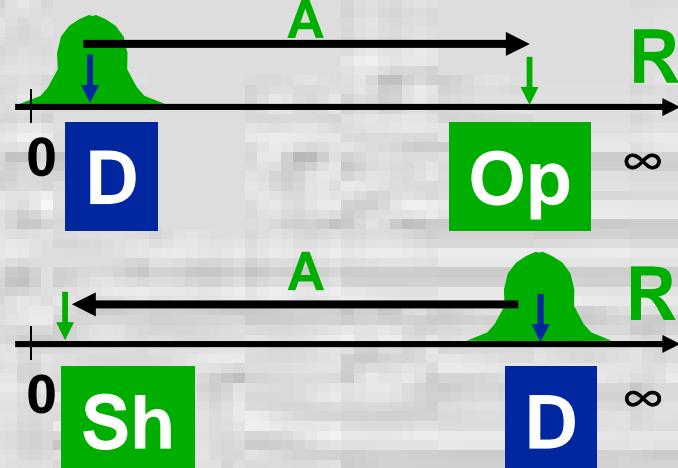


Deviation



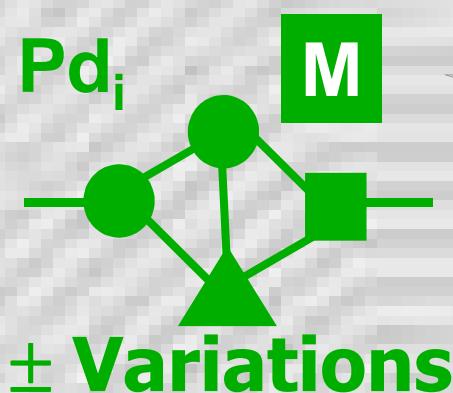
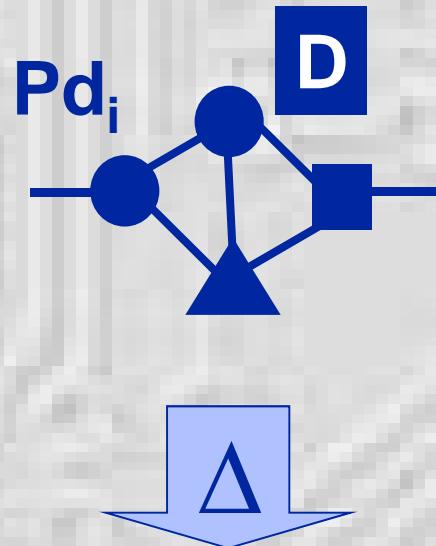
Spot

Small & Systematic



Large & Scarce

Fund. Props

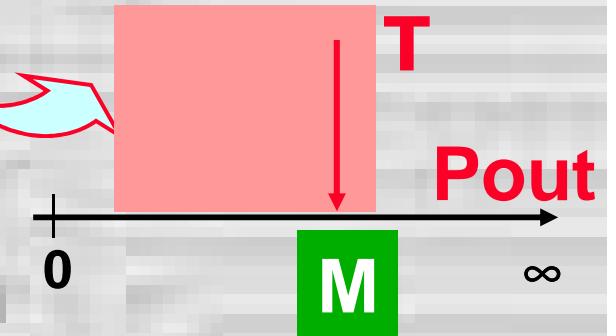
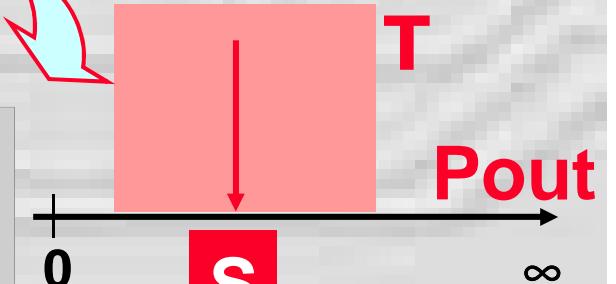
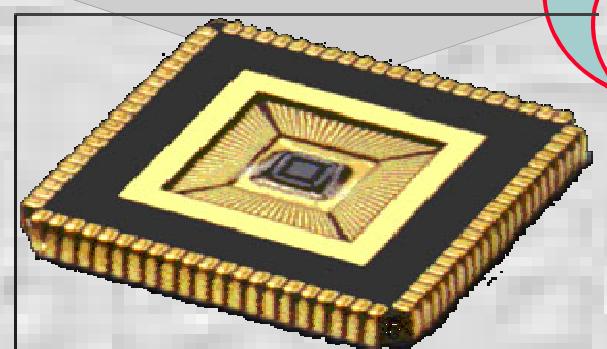


A screenshot of HDL (Hardware Description Language) code in a software interface. The code defines a process block:

```
process begin
  wait until not CLOCK'stable
  and CLOCK=1;
  if(ENABLE='1') then
    TOGGLE<= not TOGGLE;
  end if;
end process;
```

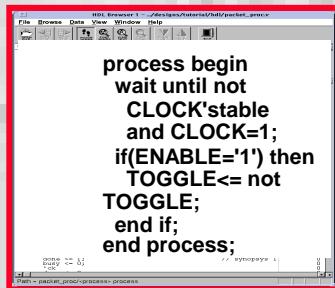


$$Se = \Delta P_{out} / \Delta P_{di}$$



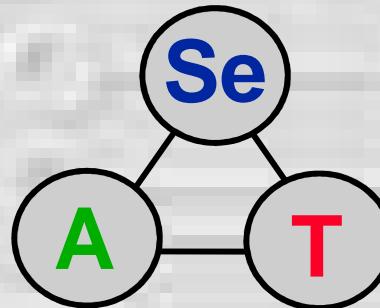
Fund. Props

Specification ?



```

process begin
  wait until not
    CLOCK'stable
    and CLOCK=1;
  if(ENABLE='1') then
    TOGGLE<= not
    TOGGLE;
  end if;
end process;
  
```



→ Amplitude : A / D ⇒ F

$$A * Se < T ?$$

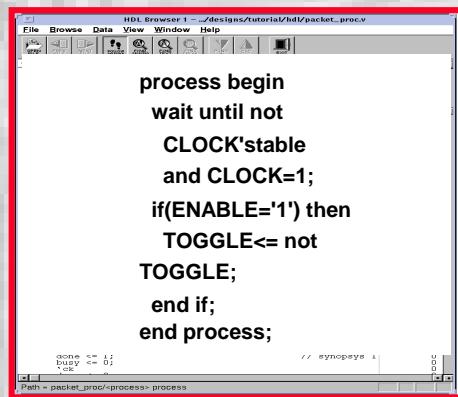
→ Tolerance : Po / S ± T

$$A < T / Se ?$$

→ Sensitivity : $Se = \frac{\Delta Ps}{\Delta Pdi}$

Robustness

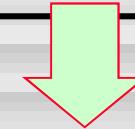
Fund. Props



```
process begin
  wait until not
  CLOCK'stable
  and CLOCK=1;
  if(ENABLE='1') then
    TOGGLE<= not
  TOGGLE;
  end if;
end process;
```

Specification ?

A < T / Se ?



Robustness

Low T/Se

Deviations
Small
Systematic

Spot
Large
Scarce

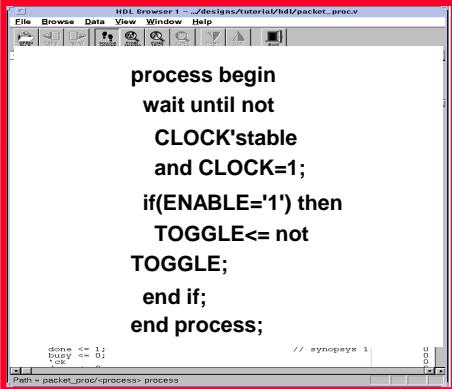
High T/Se

Spot
Large
Scarce

Fund. Props

IN2P3

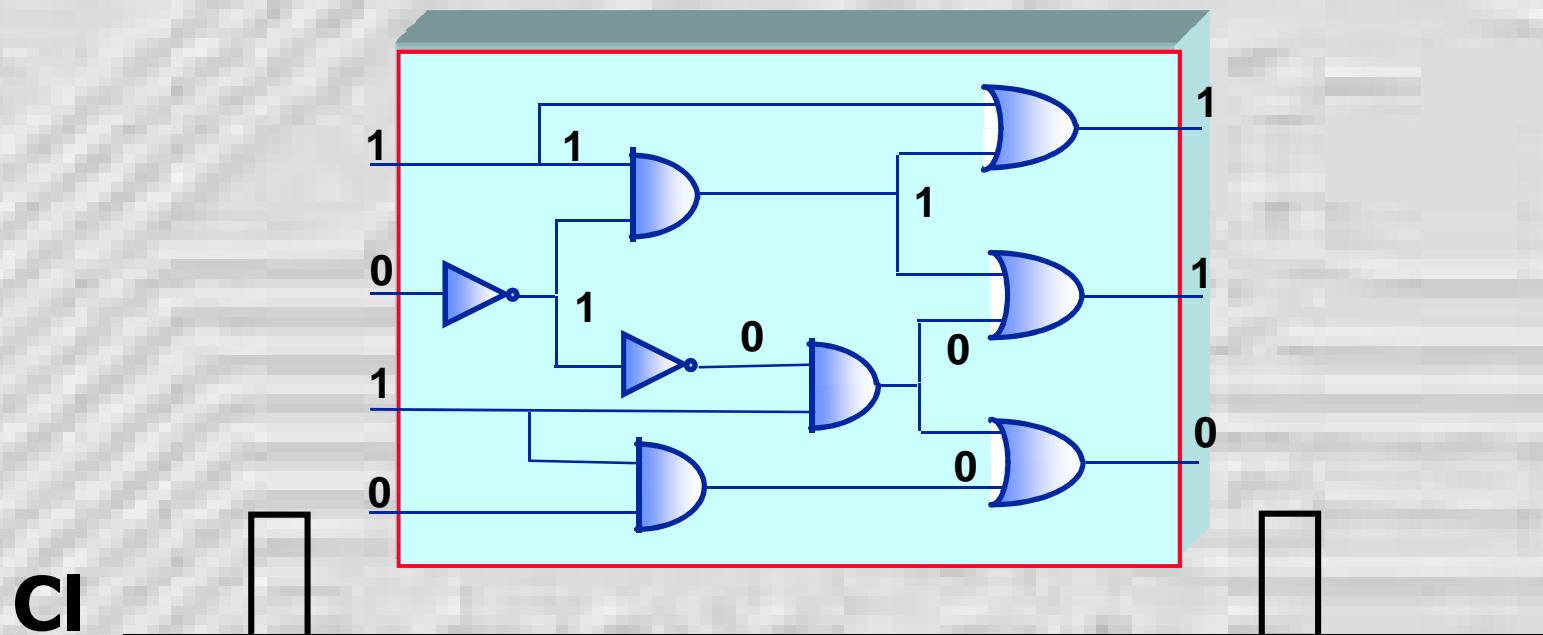
Digital



```
process begin
  wait until not
    CLOCK'stable
    and CLOCK=1;
  if(ENABLE='1') then
    TOGGLE<= not
    TOGGLE;
  end if;
end process;
```

Specification ?

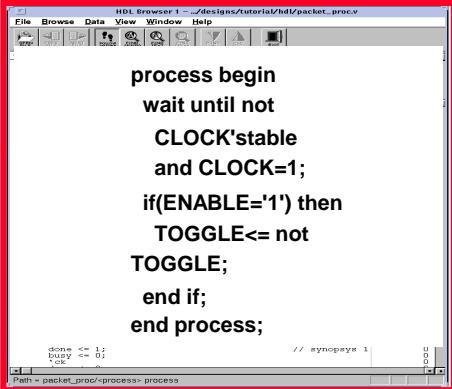
- Logic
- Timing



Fund. Props

IN2P3

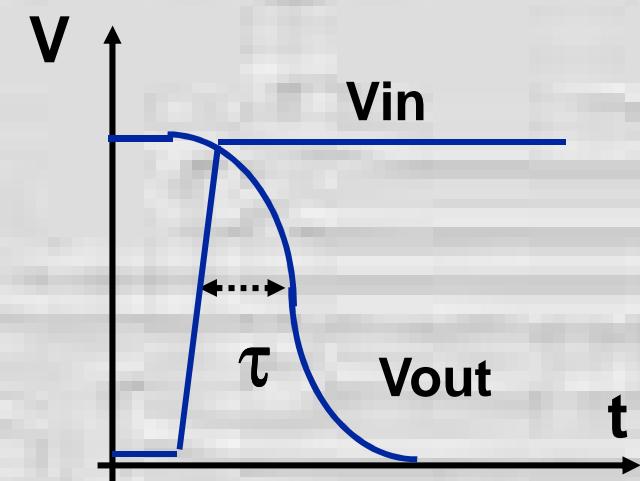
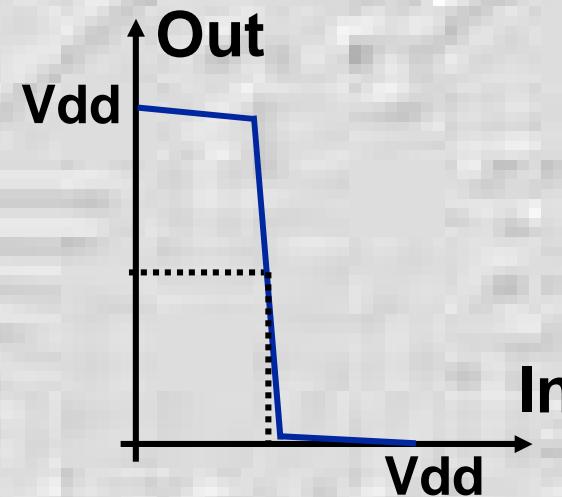
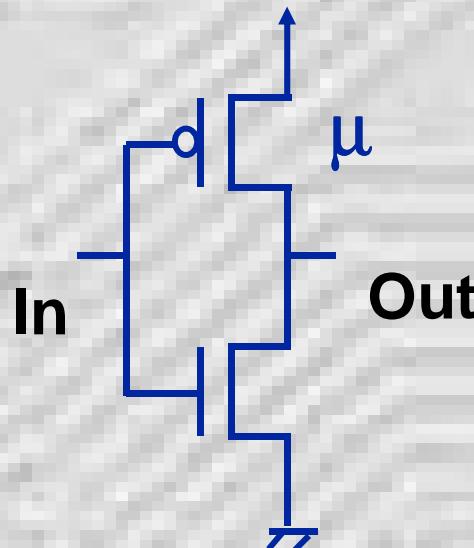
Digital



```
process begin
  wait until not
    CLOCK'stable
    and CLOCK=1;
  if(ENABLE='1') then
    TOGGLE<= not
    TOGGLE;
  end if;
end process;
```

Specification ?

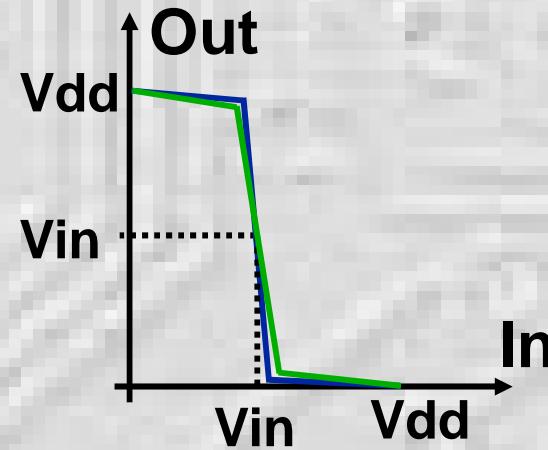
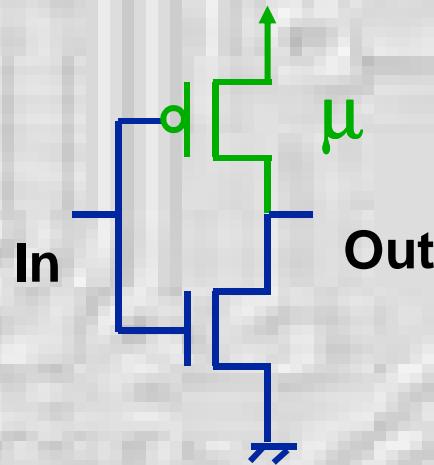
- Logic
- Timing



Fund. Props

IN2P3

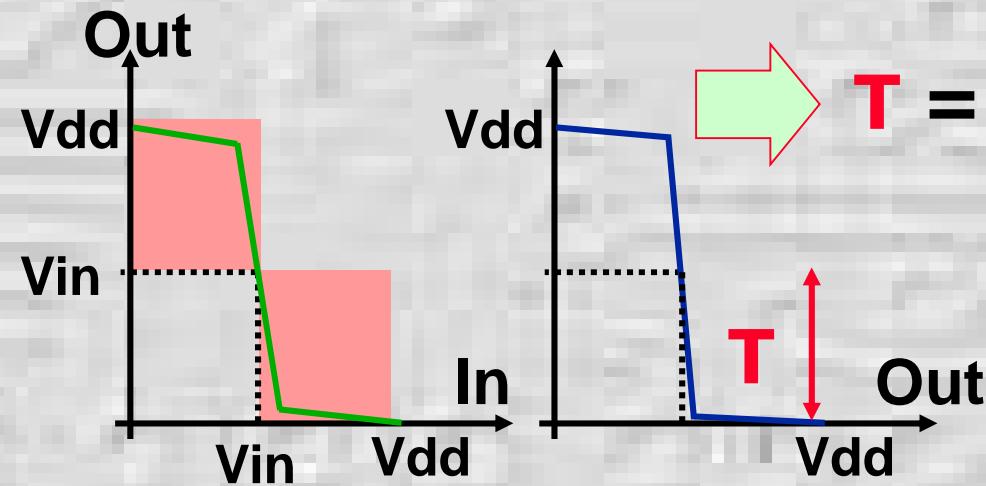
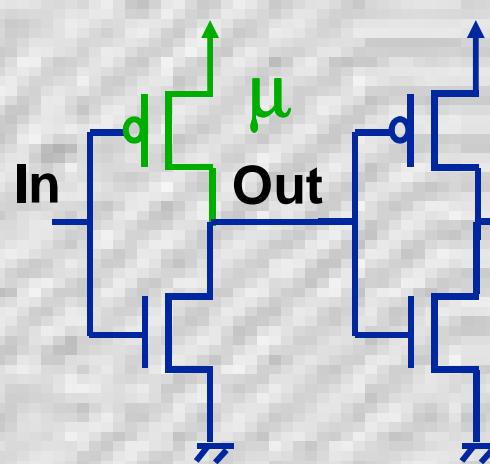
Digital



$$Se = \frac{\Delta P_s}{\Delta P_{di}}$$

Very High T/Se

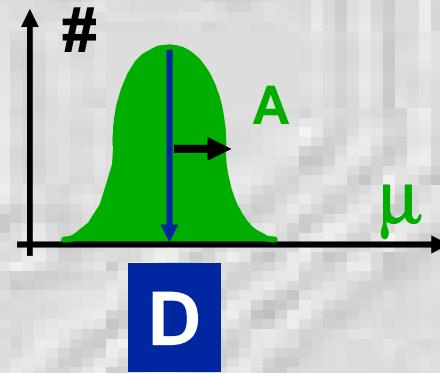
Circuit Indpt



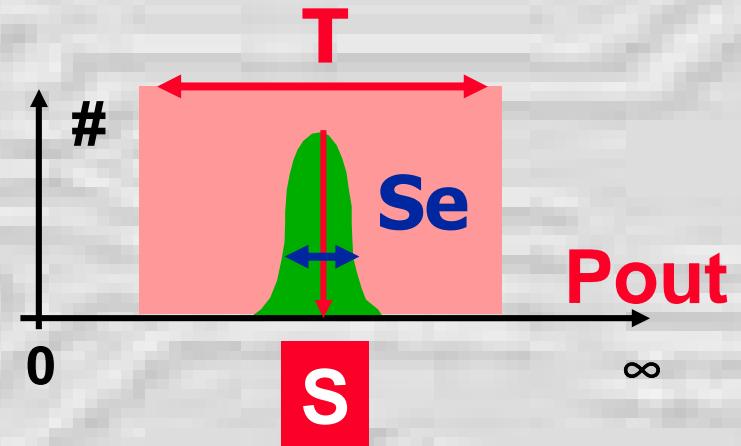
Fund. Props

IN2P3

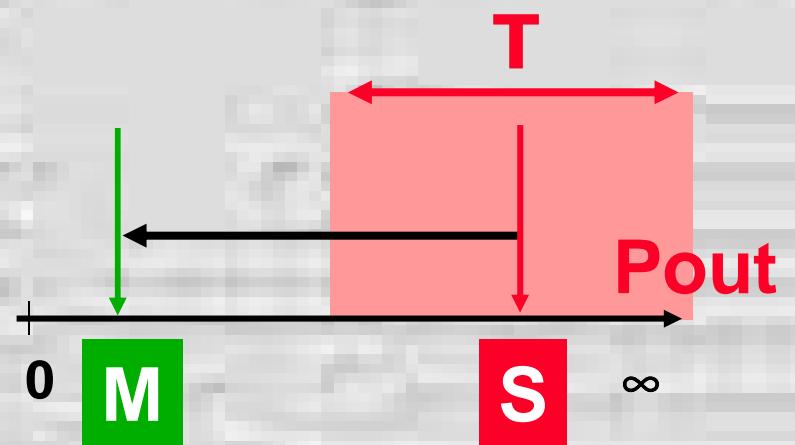
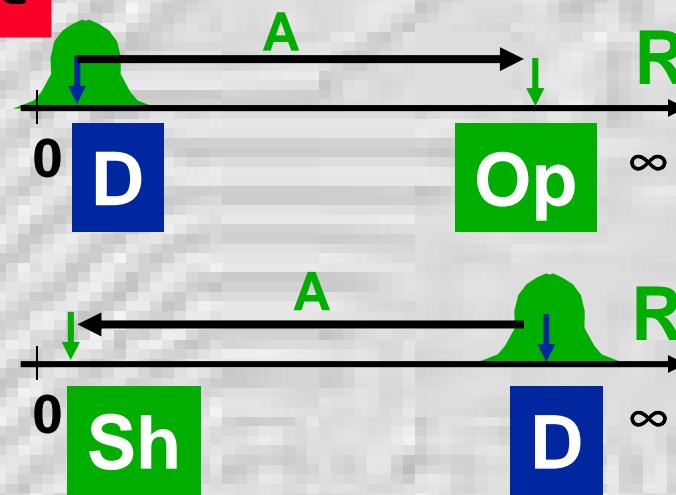
Deviation



Digital



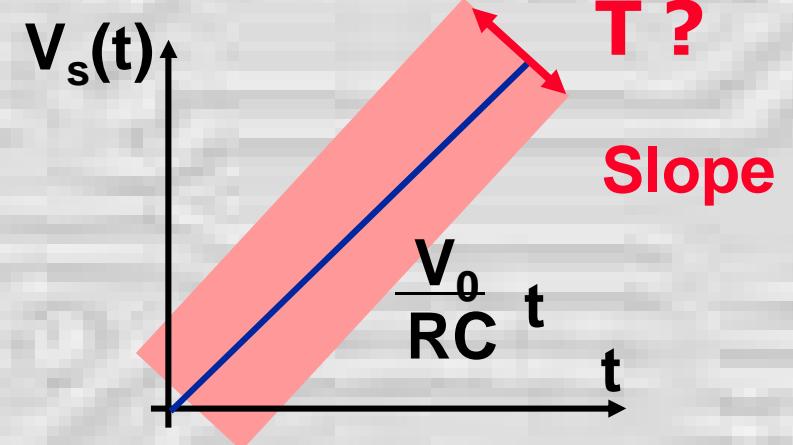
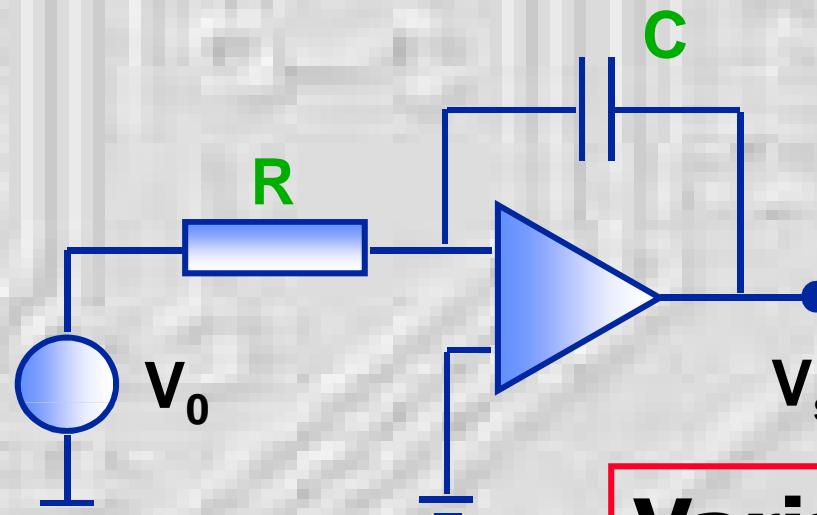
Spot



Fund. Props

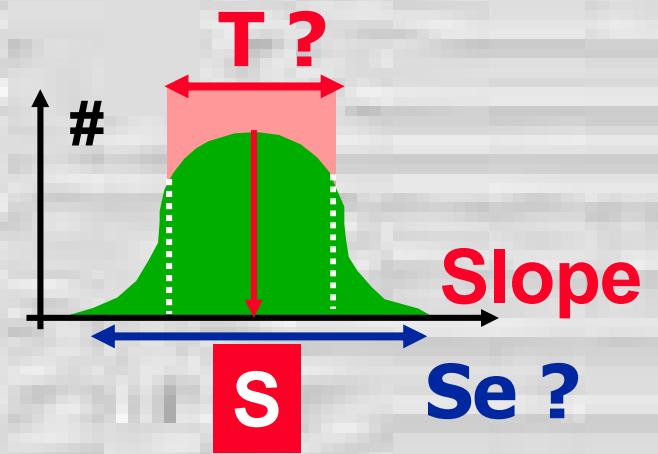
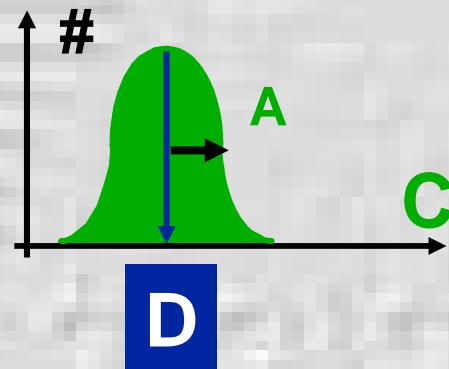
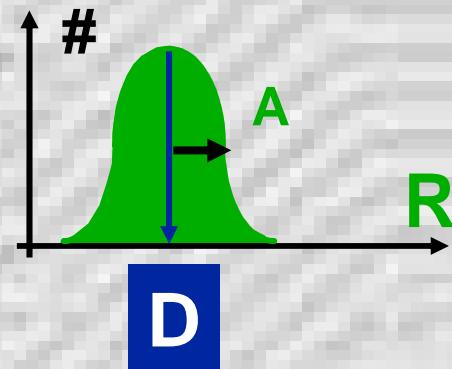
IN2P3

Analog



Variable T/Se

Circuit Dpt



Fund. Props

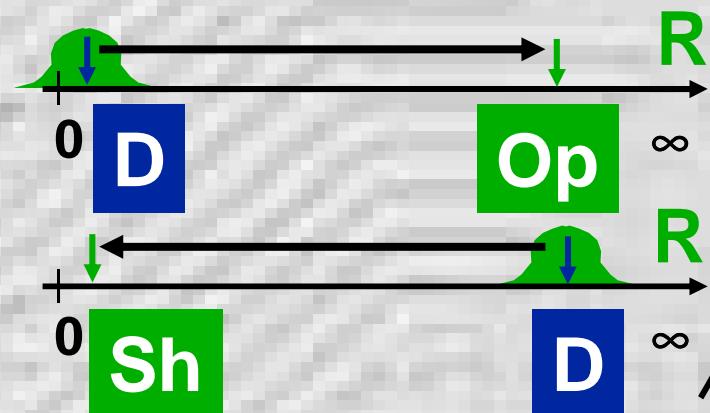
Digital

High T/Se

Spots

Large & Sc.

Defect Oriented Test

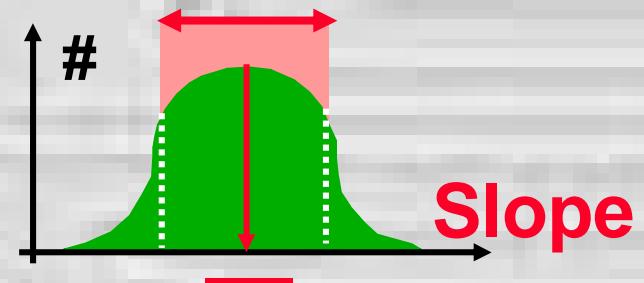


Analog

Low T/Se

Deviations Small & Syst.
Spots Large & Sc.

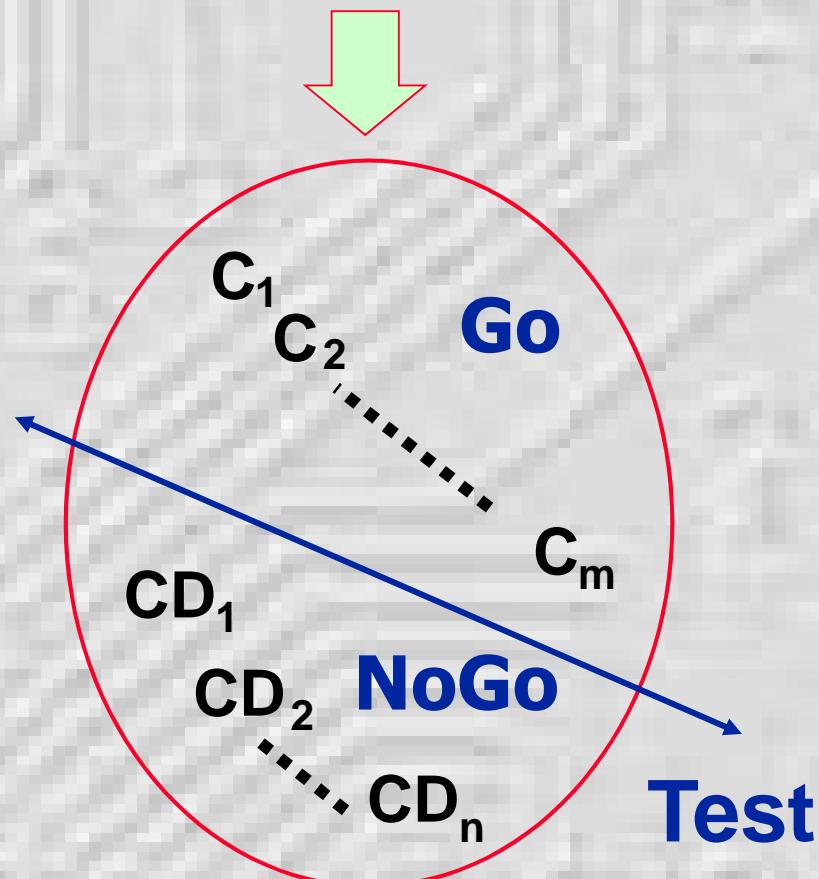
Spec Oriented Test



Timing

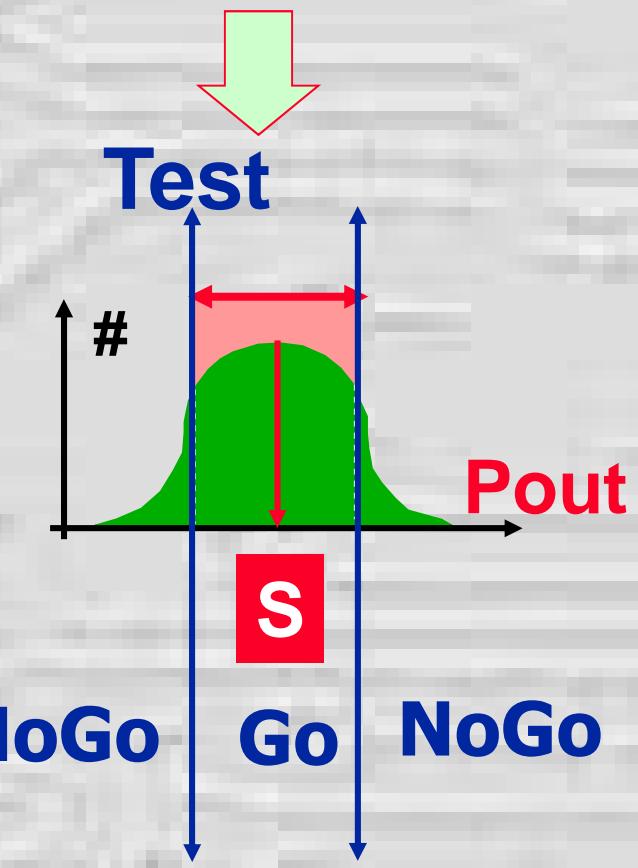
Digital

Defect Oriented Test



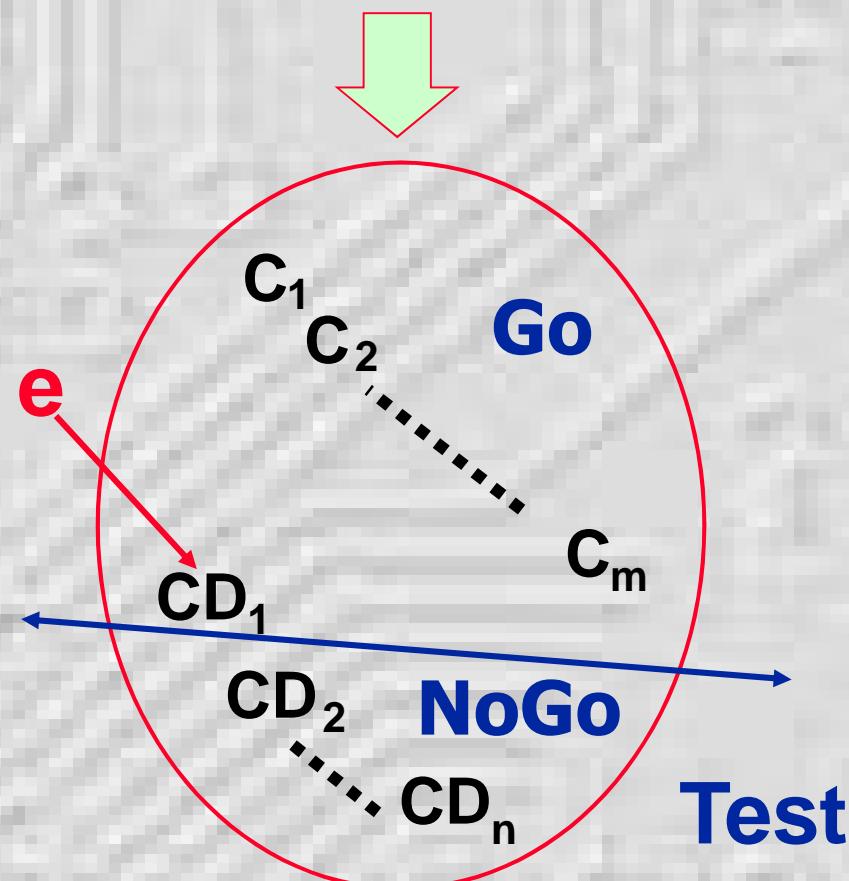
Analog

Spec Oriented Test



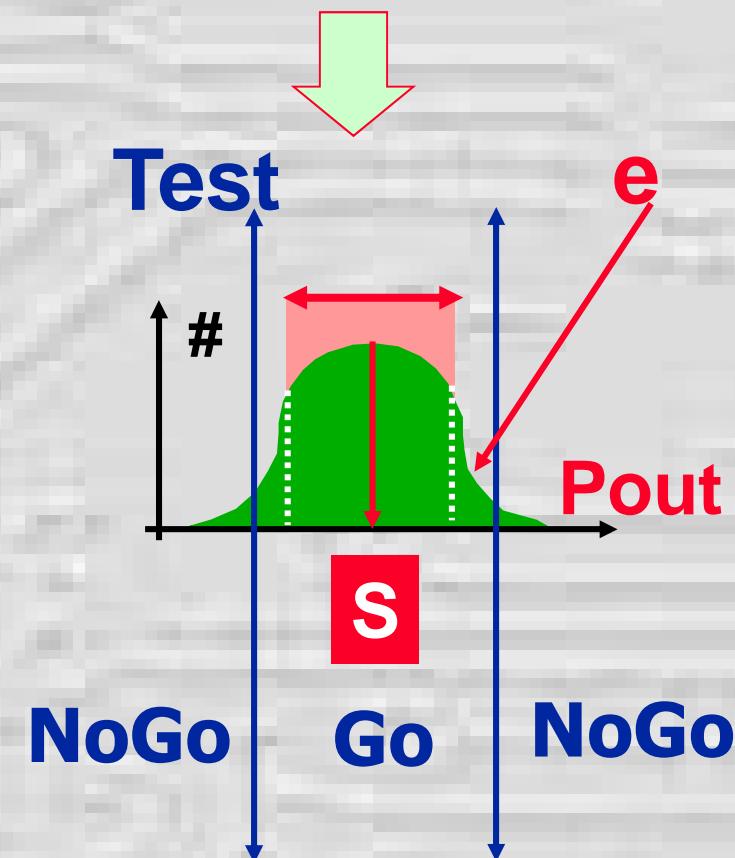
Digital

Defect Oriented Test



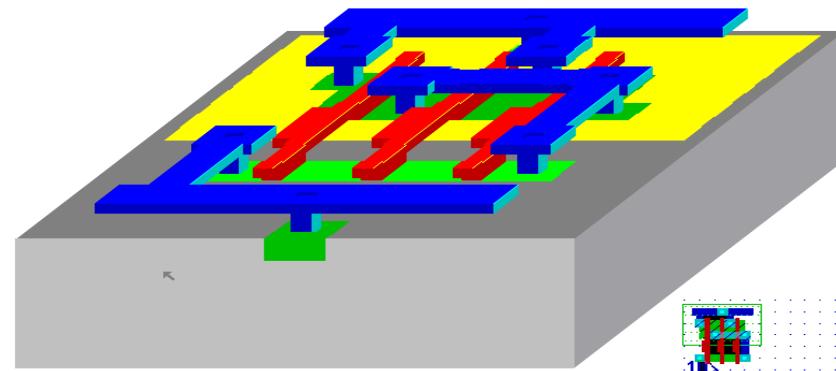
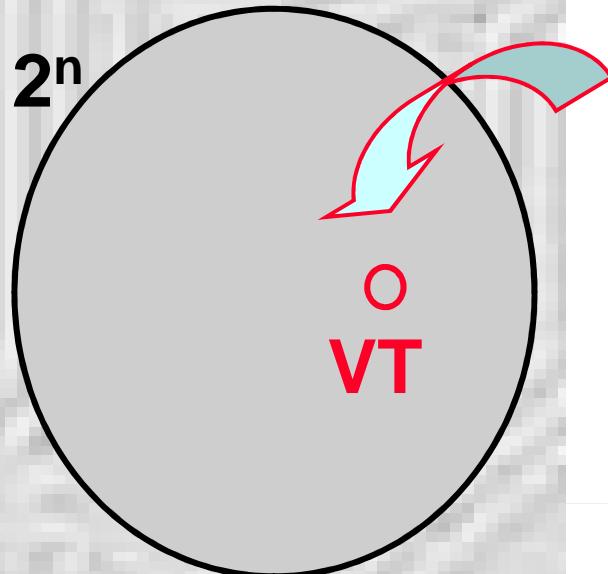
Analog

Spec Oriented Test



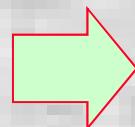
Digital Approach

Digital Approach



Spot-Free Digital Circuit \Leftrightarrow In Specification

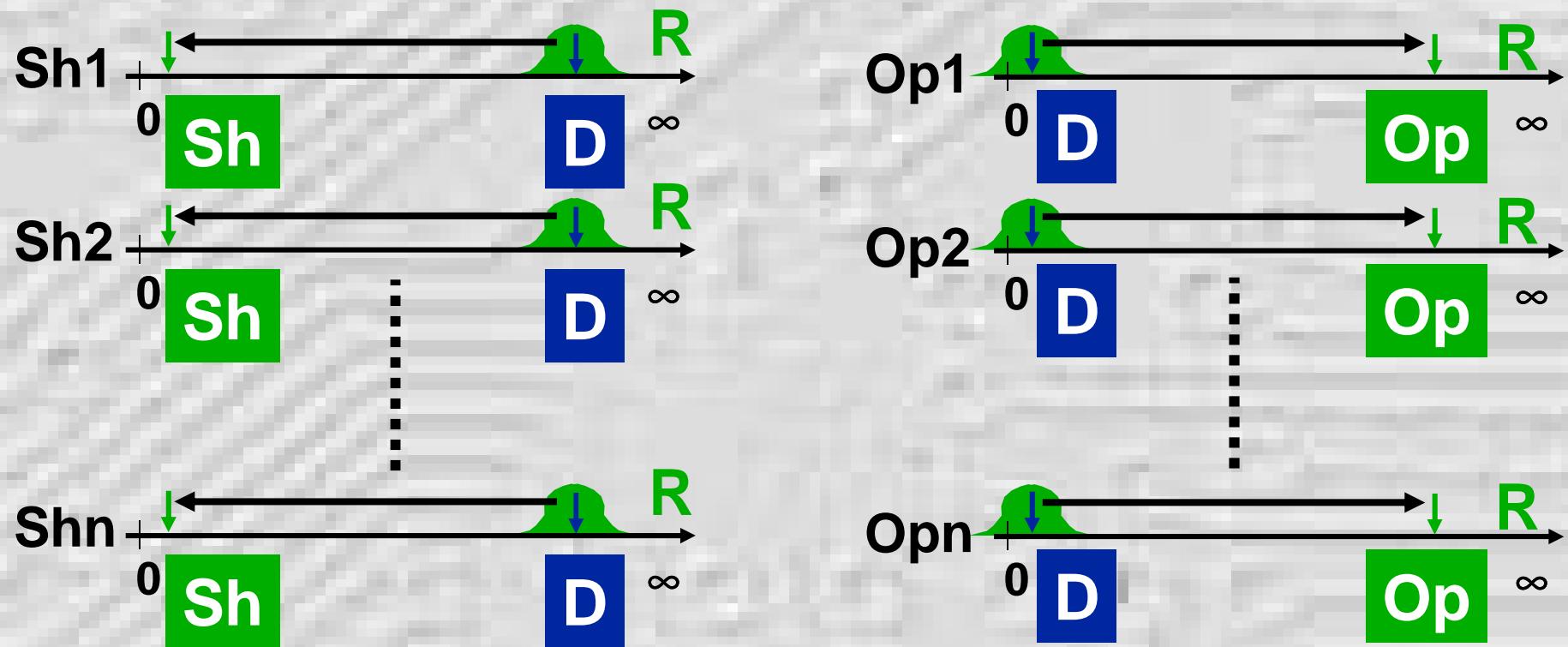
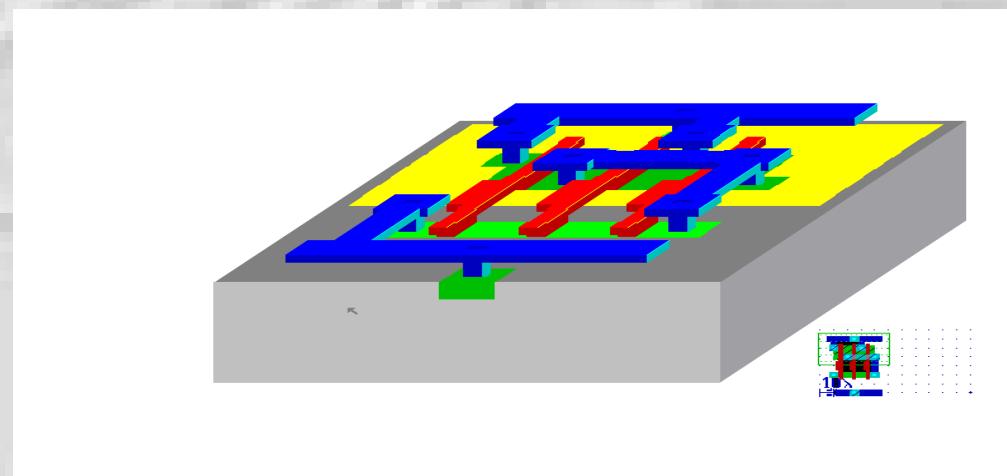
For each possible spot
Compute a stimuli
that reveals its presence



Test Pattern
List

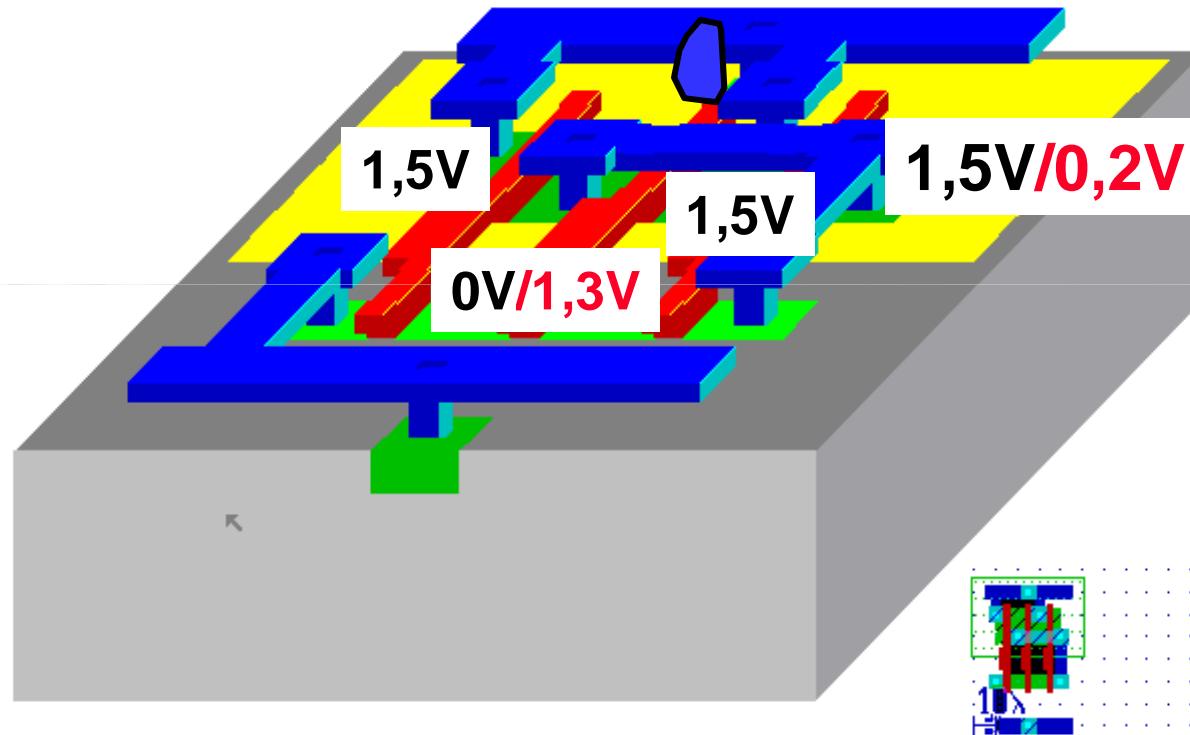
Digital Approach

IN2P3

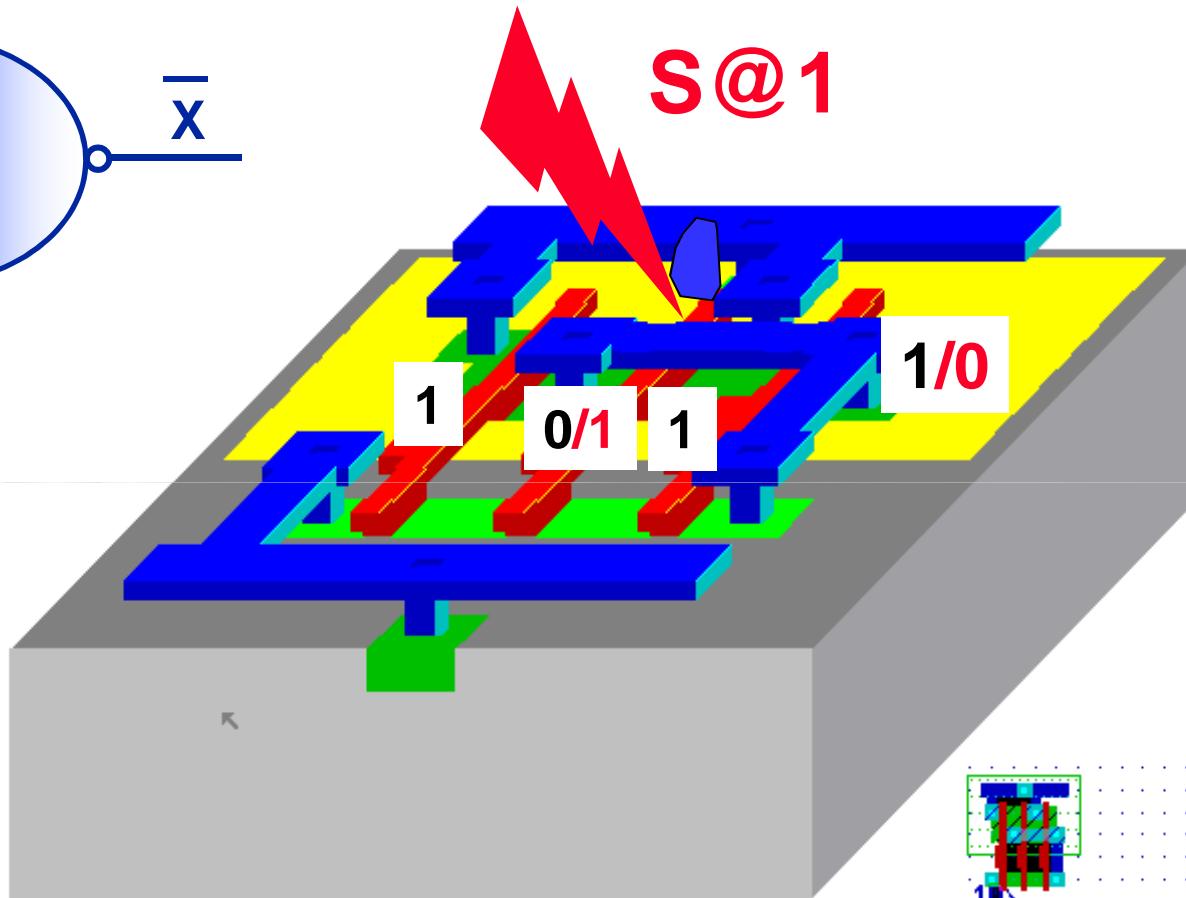
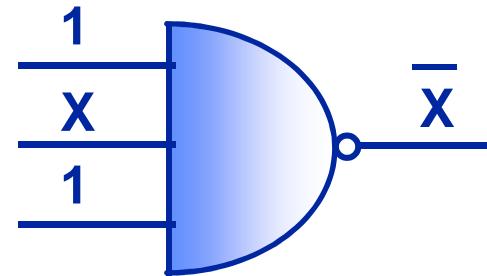


Digital Approach

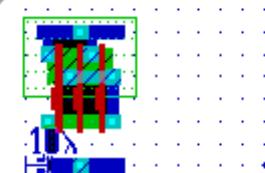
IN2P3



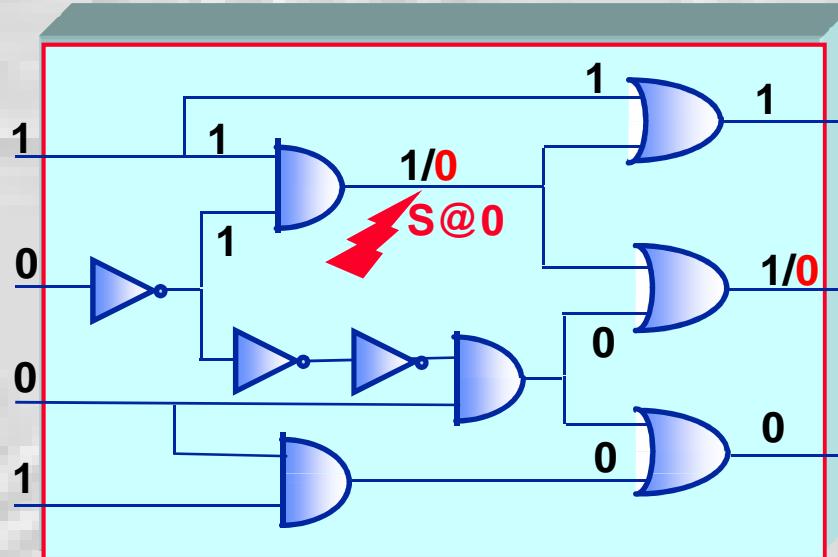
Digital Approach



Spot \Leftrightarrow Fault Model
- S@0
- S@1



Digital Approach



Cost

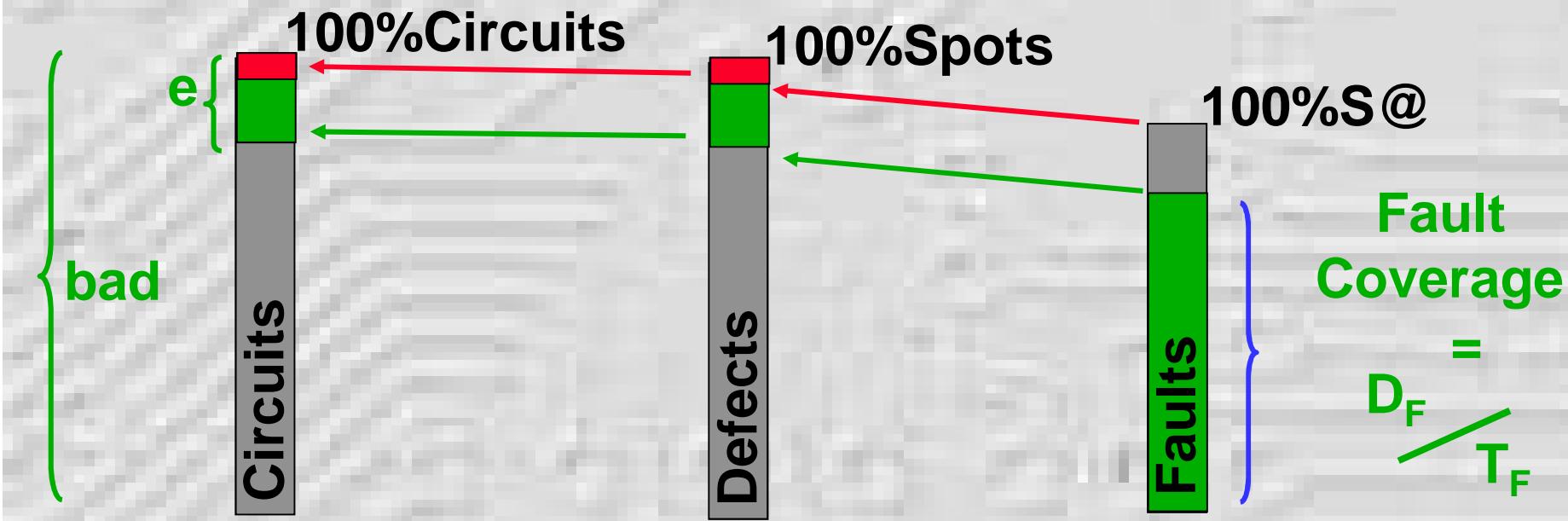
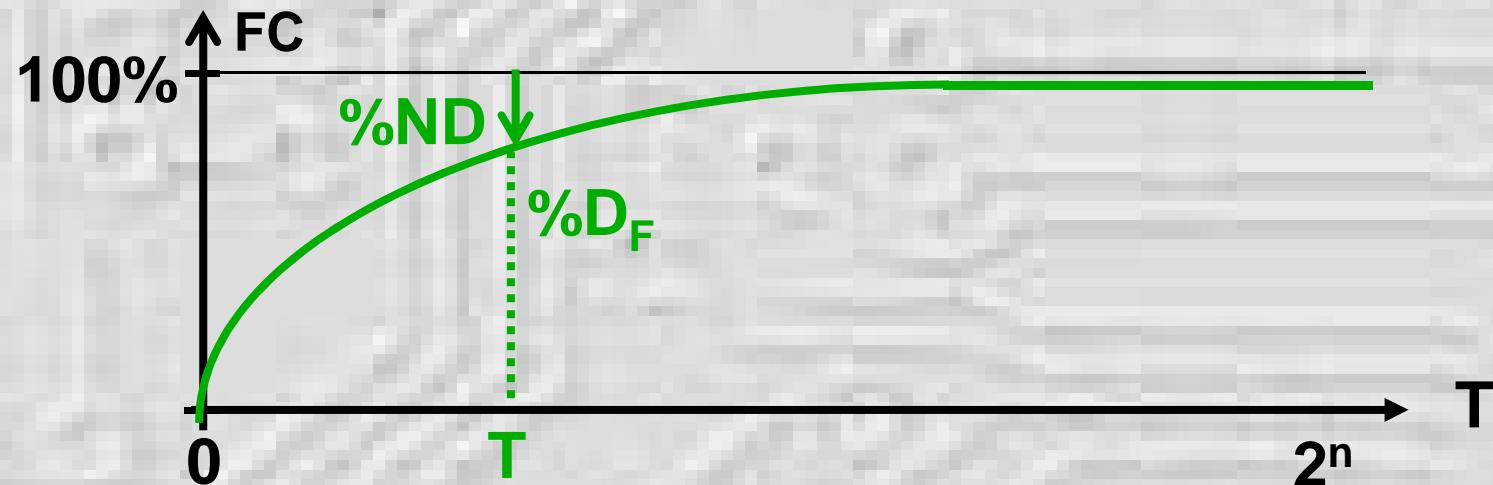
- 10^6 gates
- 10^6 nodes
- 10^6 S@0
- 10^6 S@1
- $2 \cdot 10^6$ vectors
- 100Mhz

Physical Structure <=> Logical Structure

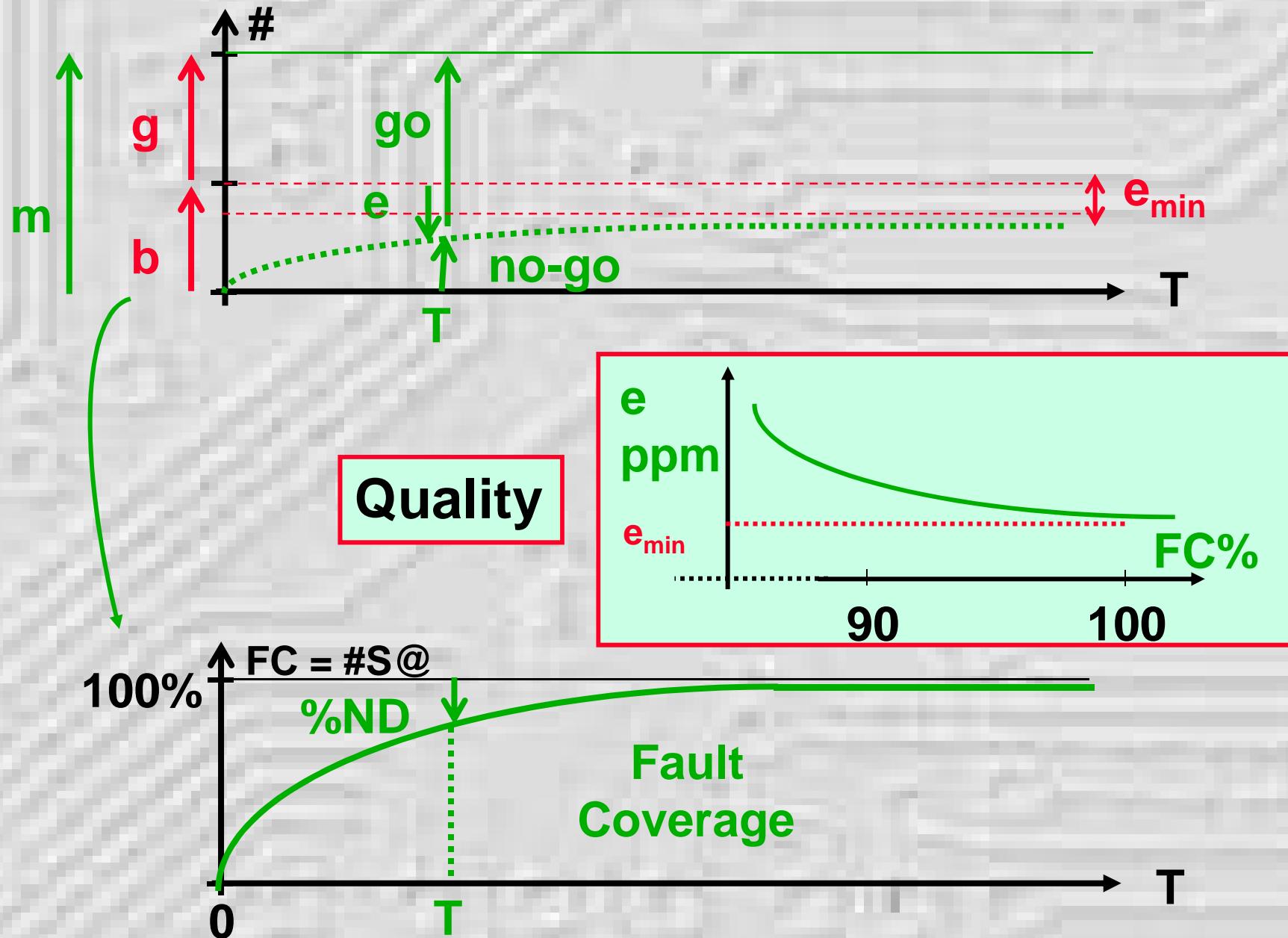
- Each Logic node S@0
- Each Logic node S@1
- TPG

Digital Approach

IN2P3



Digital Approach

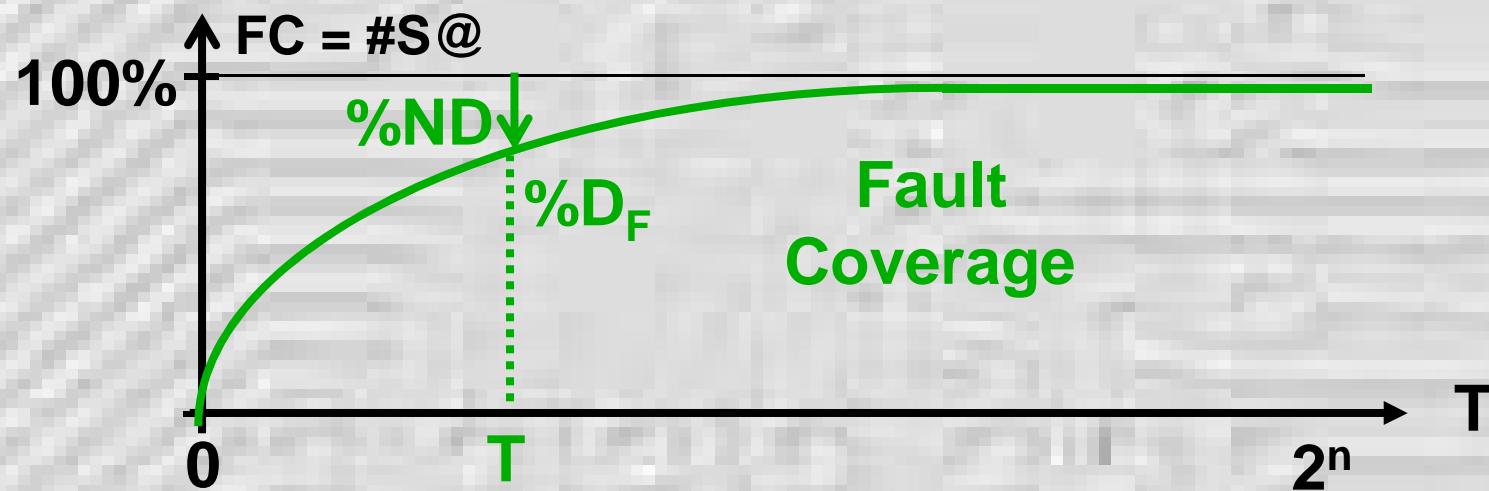


Digital Approach



I) Criteria to stop the test generation

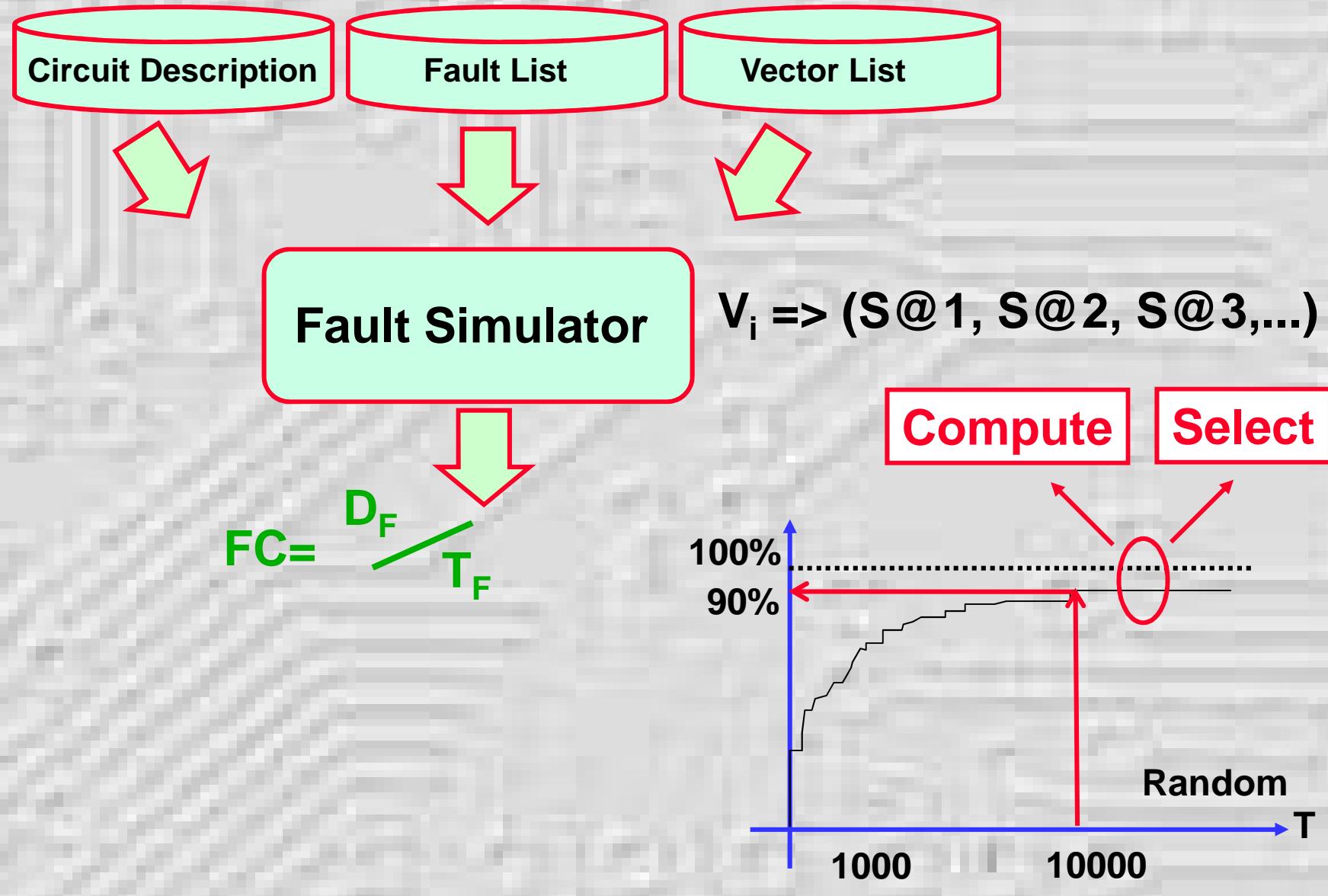
=> Estimate how many faulty circuits not yet detected (e?)



Test Generation

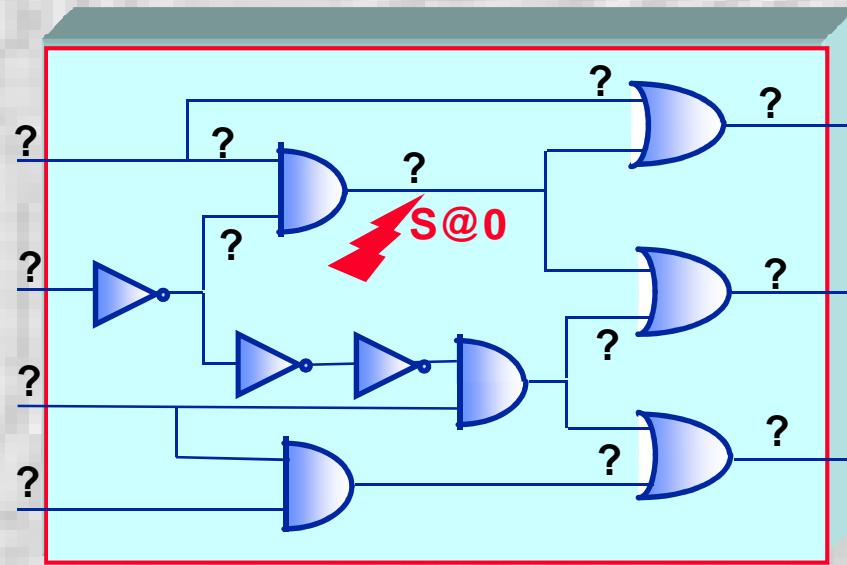
Test Generation

IN2P3

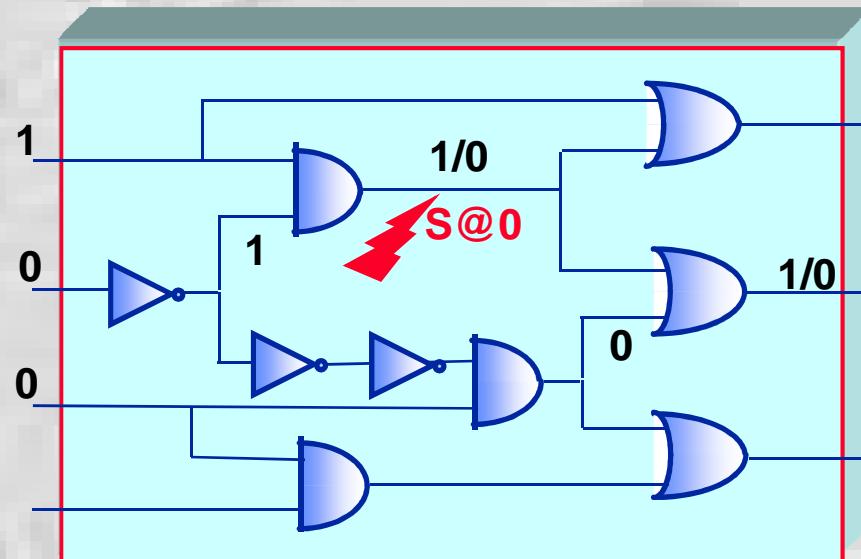


Test Generation

IN2P3

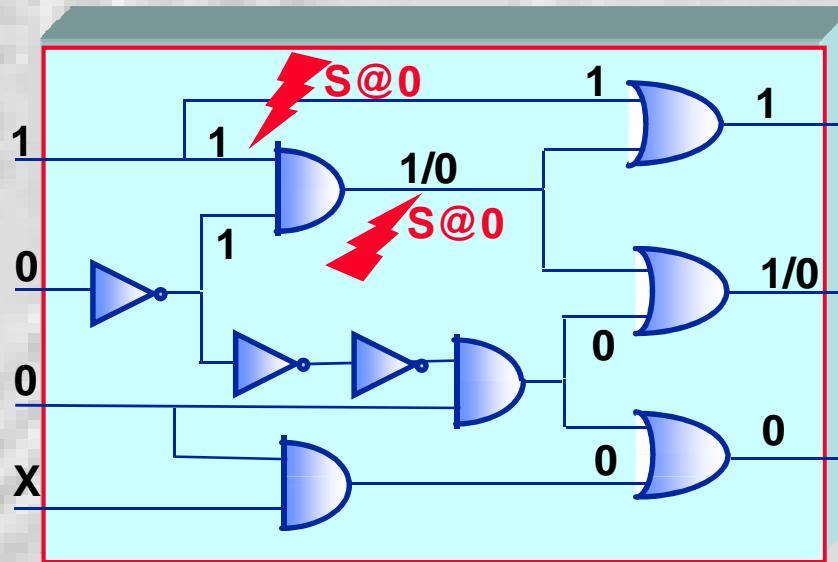


Compute \Leftrightarrow ATPG



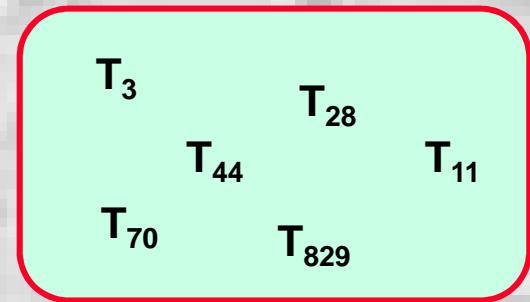
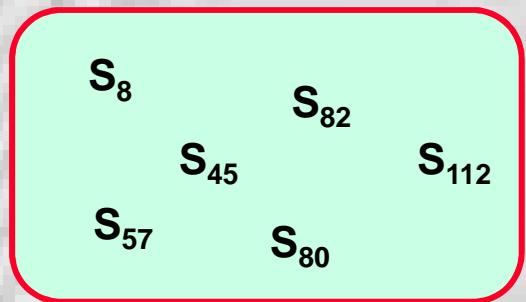
Test Generation

IN2P3



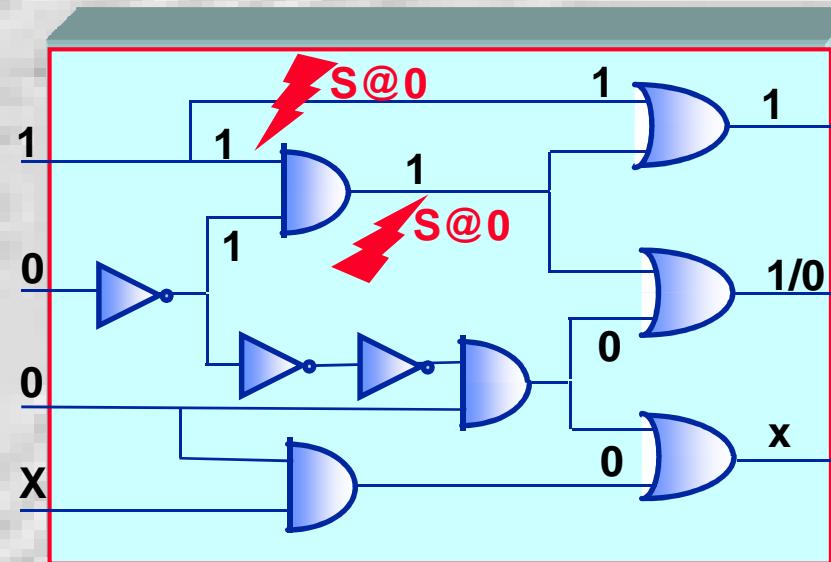
T_9

S_{13}



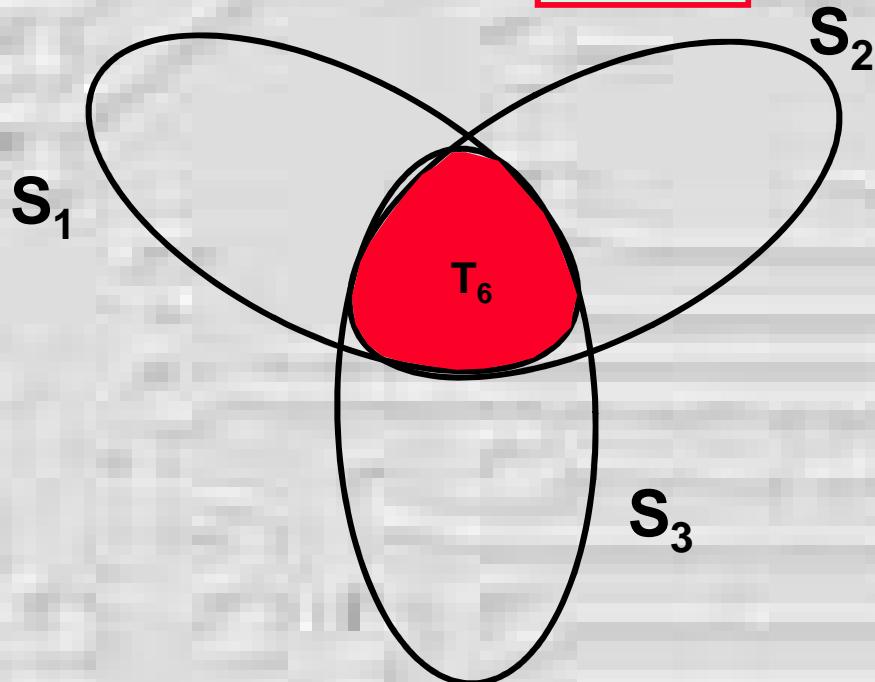
Test Generation

IN2P3



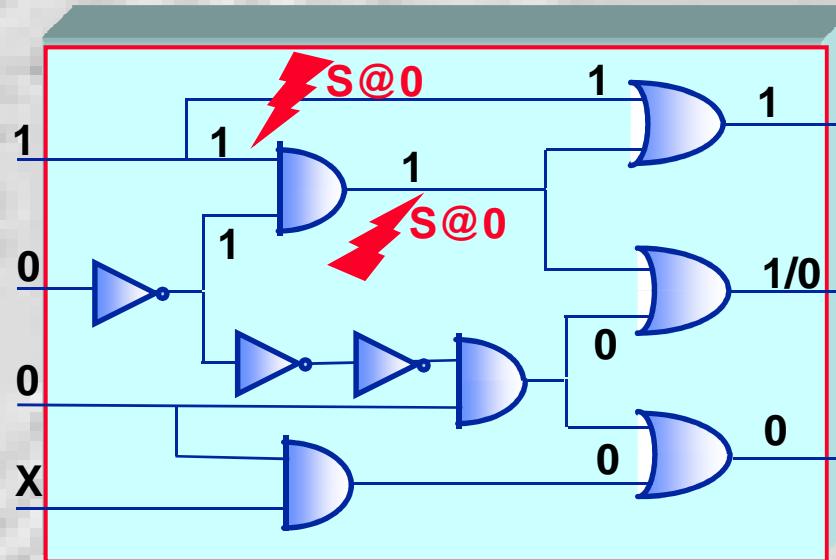
Cost

- Desired e (Application)
- Desired FC%
- Structural ATPG => Vectors
- Minimal number



Test Generation

IN2P3



FC 90%

- $S@1 \Rightarrow S1 = (T_{11} \text{ or } T_{12} \text{ or } T_{13} \dots)$
- $S@2 \Rightarrow S2 = (T_{21} \text{ or } T_{22} \text{ or } T_{23} \dots)$
- $S@3 \Rightarrow S3 = (T_{31} \text{ or } T_{32} \text{ or } T_{33} \dots)$
-

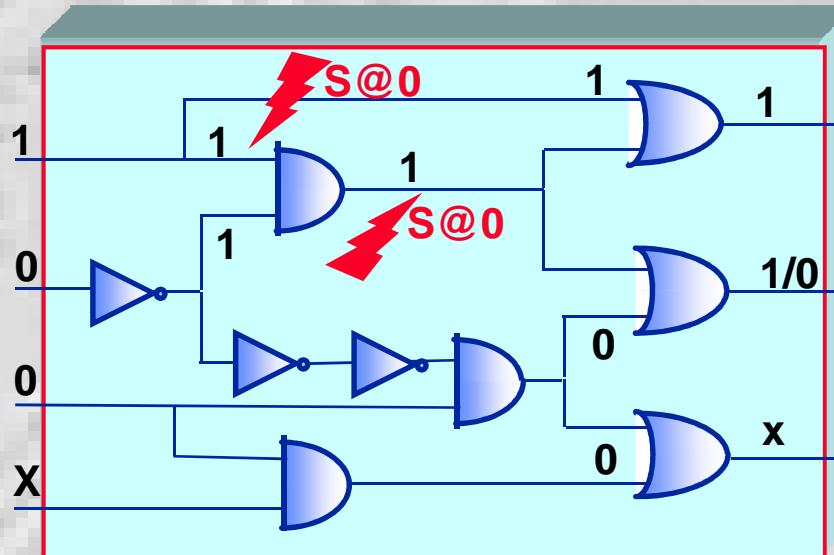
S1 and S2 and S3 and ..

$$\begin{aligned} T &= (T_1 + T_2 + T_3) (T_1) (T_2 + T_4) \\ T &= T_1 T_2 + T_1 T_2 T_3 + T_1 T_4 \\ &\quad + T_1 T_2 T_4 + T_1 T_3 T_4 \end{aligned}$$

FC 98%

Test Generation

IN2P3

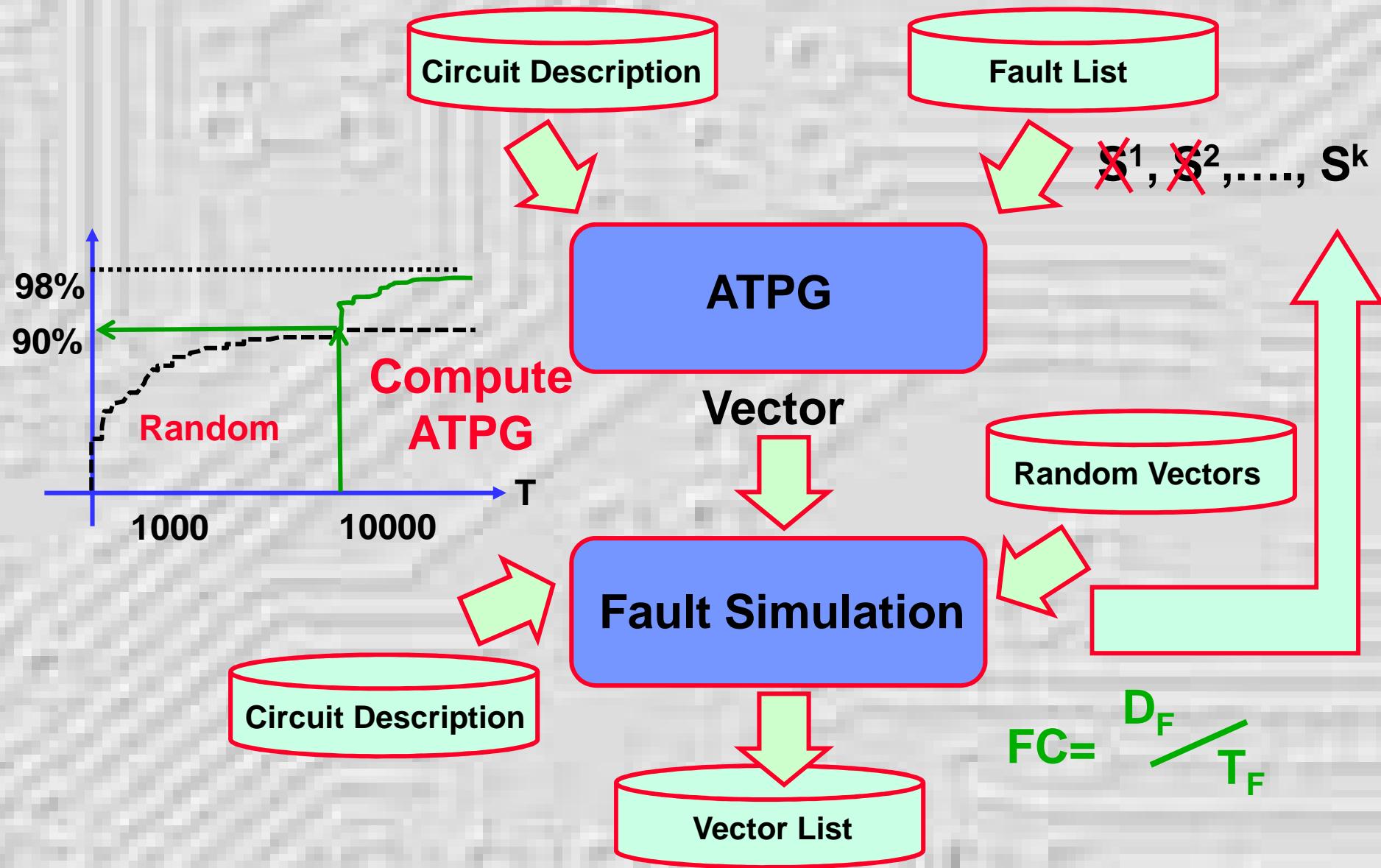


Cost

- ATPG :
 $S@1 \Rightarrow T_{11}(\text{np})$
- Fault Simulation :
 $V_{ij} \Rightarrow (S@1, S@2, S@3, S@4 \dots)(\text{ok})$

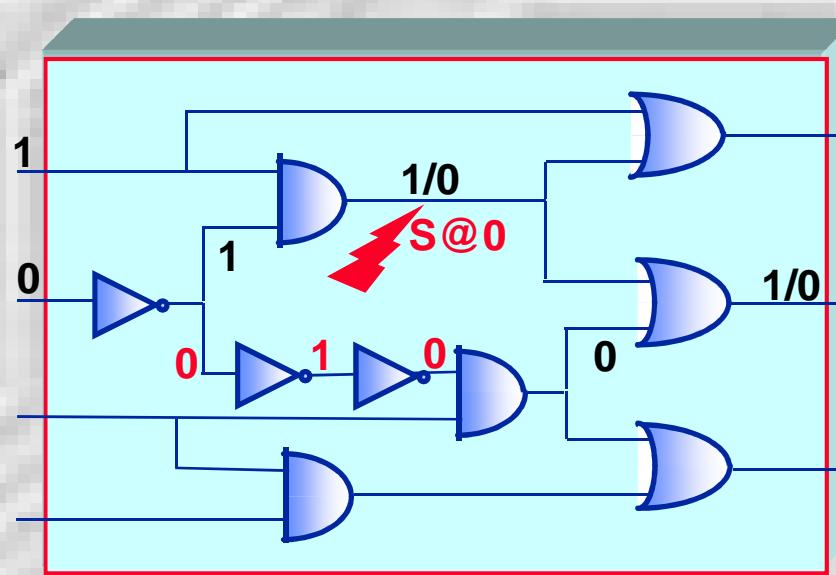
Test Generation

IN2P3



Test Generation

IN2P3



- Backward justification
 - Conflict
 - Backtrack
-
- Limited number Backtrack
 -

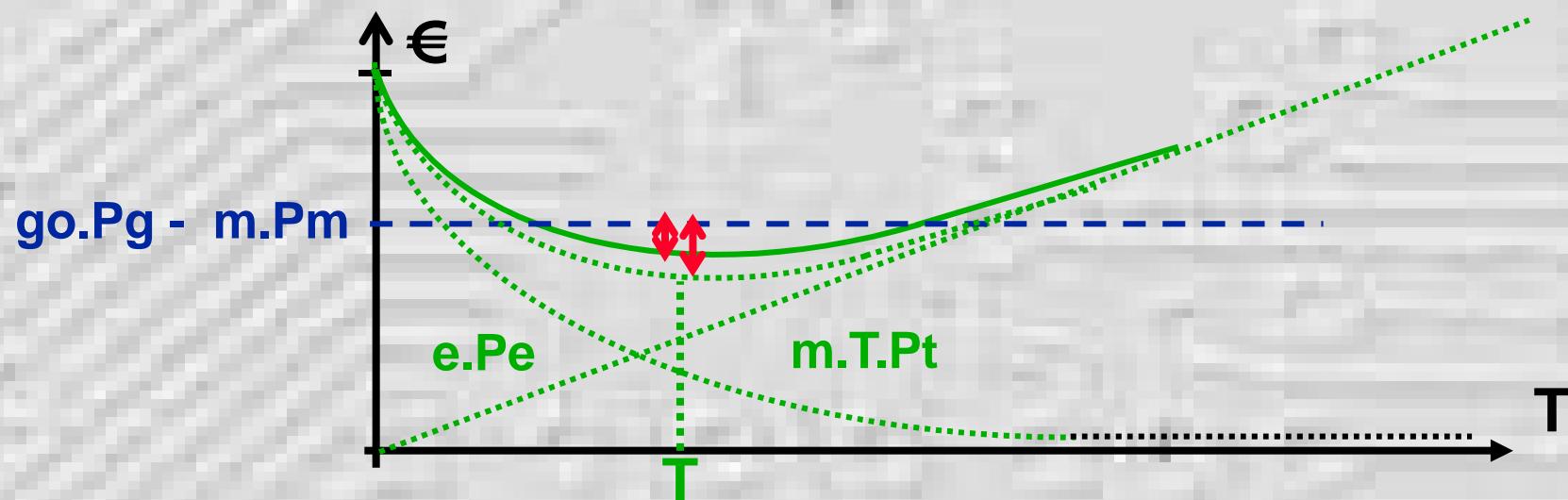
Test Generation

IN2P3

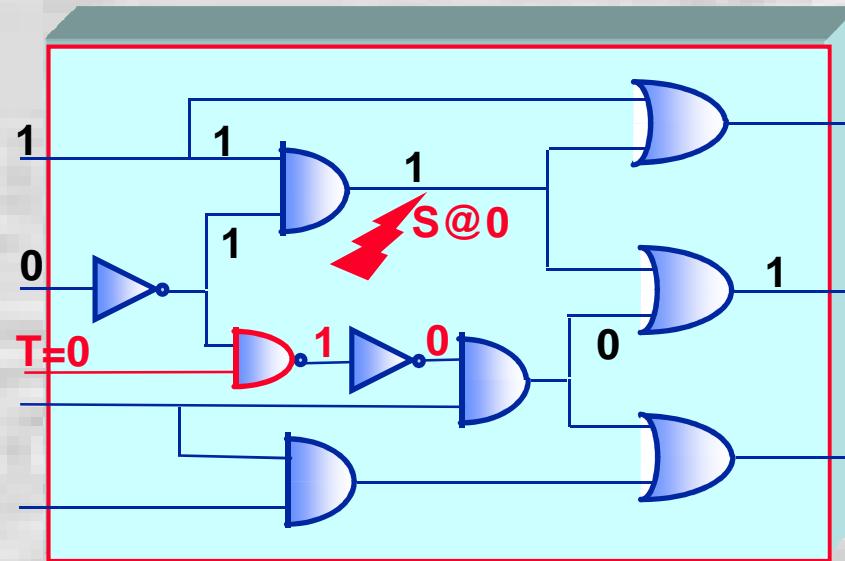
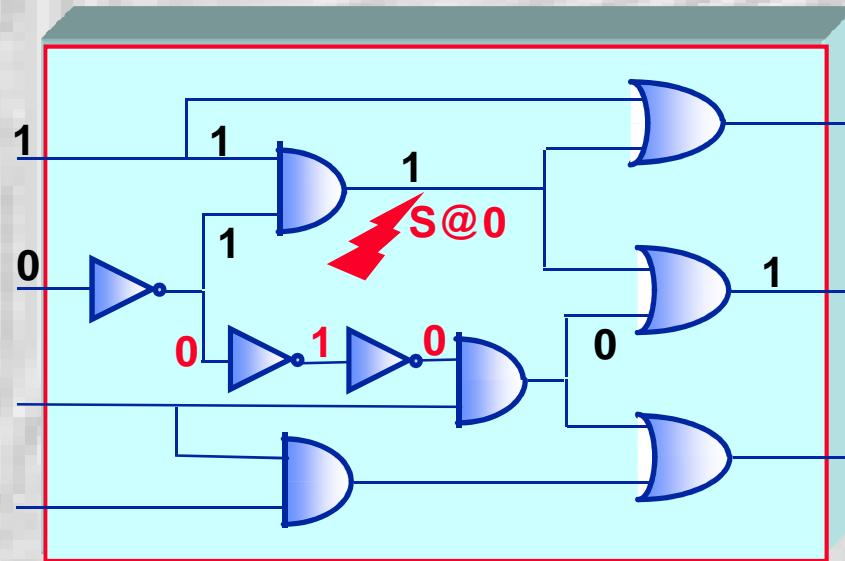


II) Criteria to optimize the test generation

=> Estimate how many faulty circuits are detected by each vector



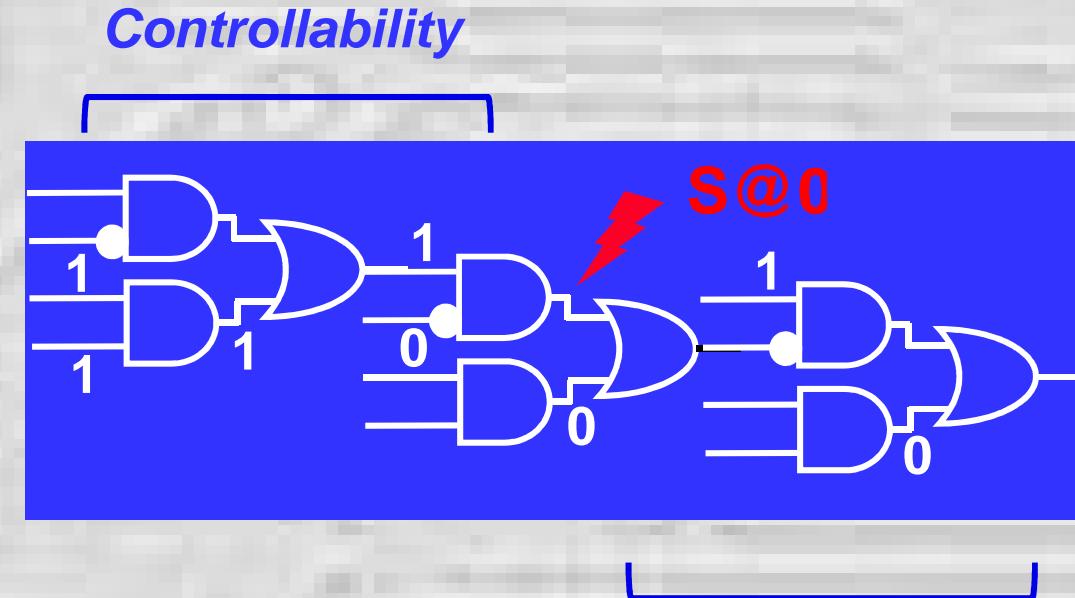
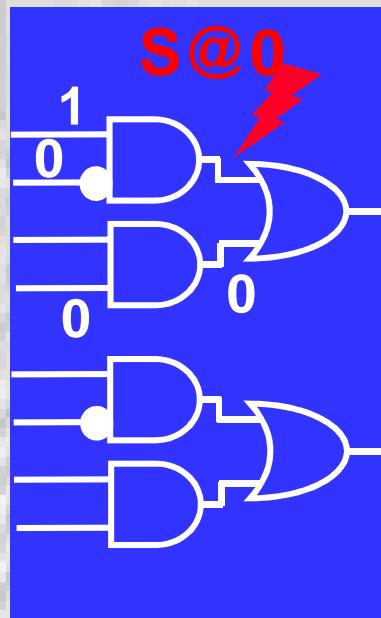
*Design
For
Testability*



- ATPG / Backtrack
 - FC < Desired FC (98%)
 - Modify the Structure

Design For Test

Combinational Logic

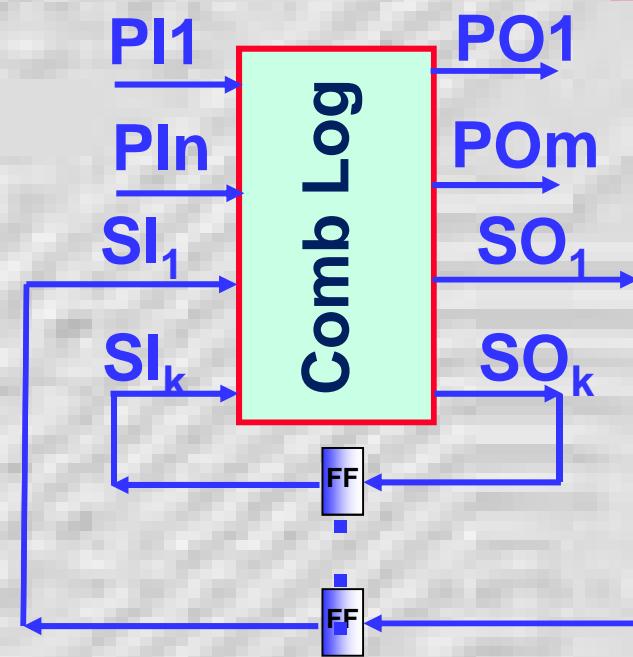
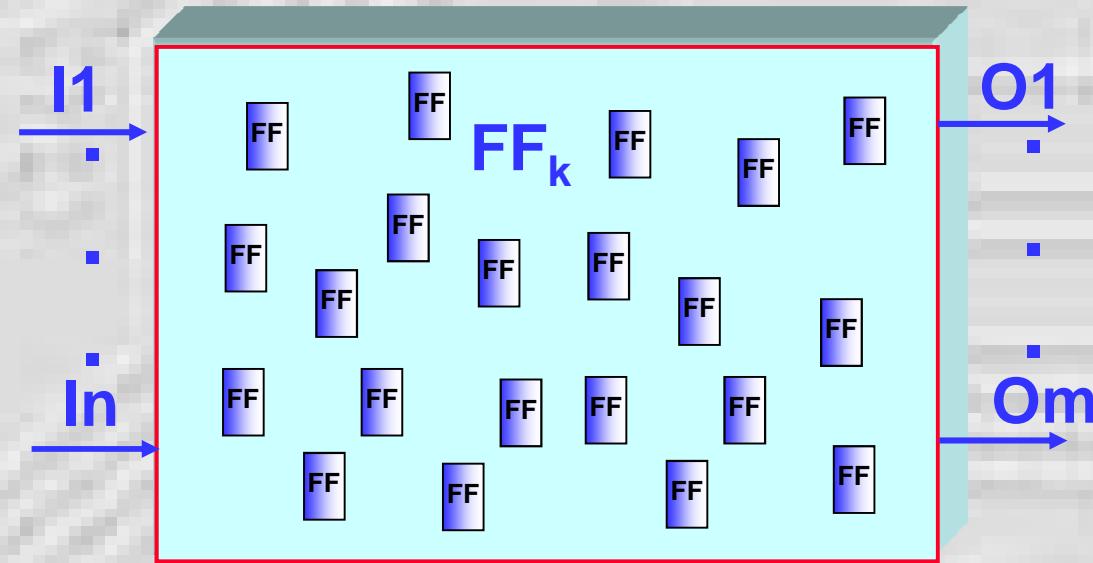


Observability

Structured DFT

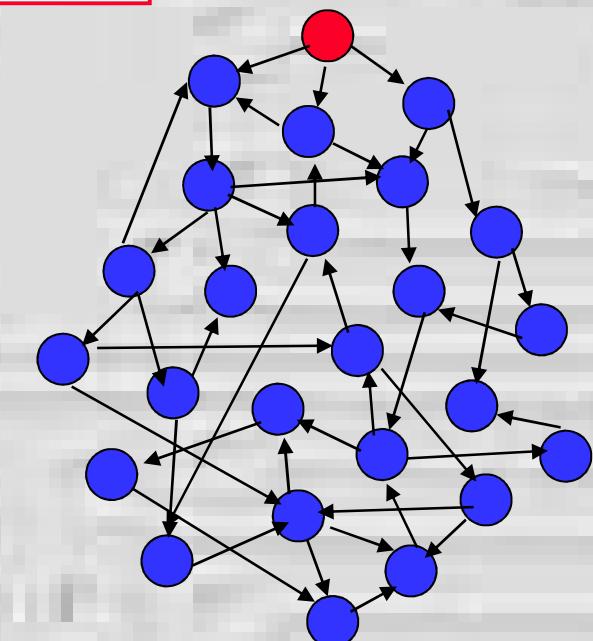
IN2P3

Sequential Logic

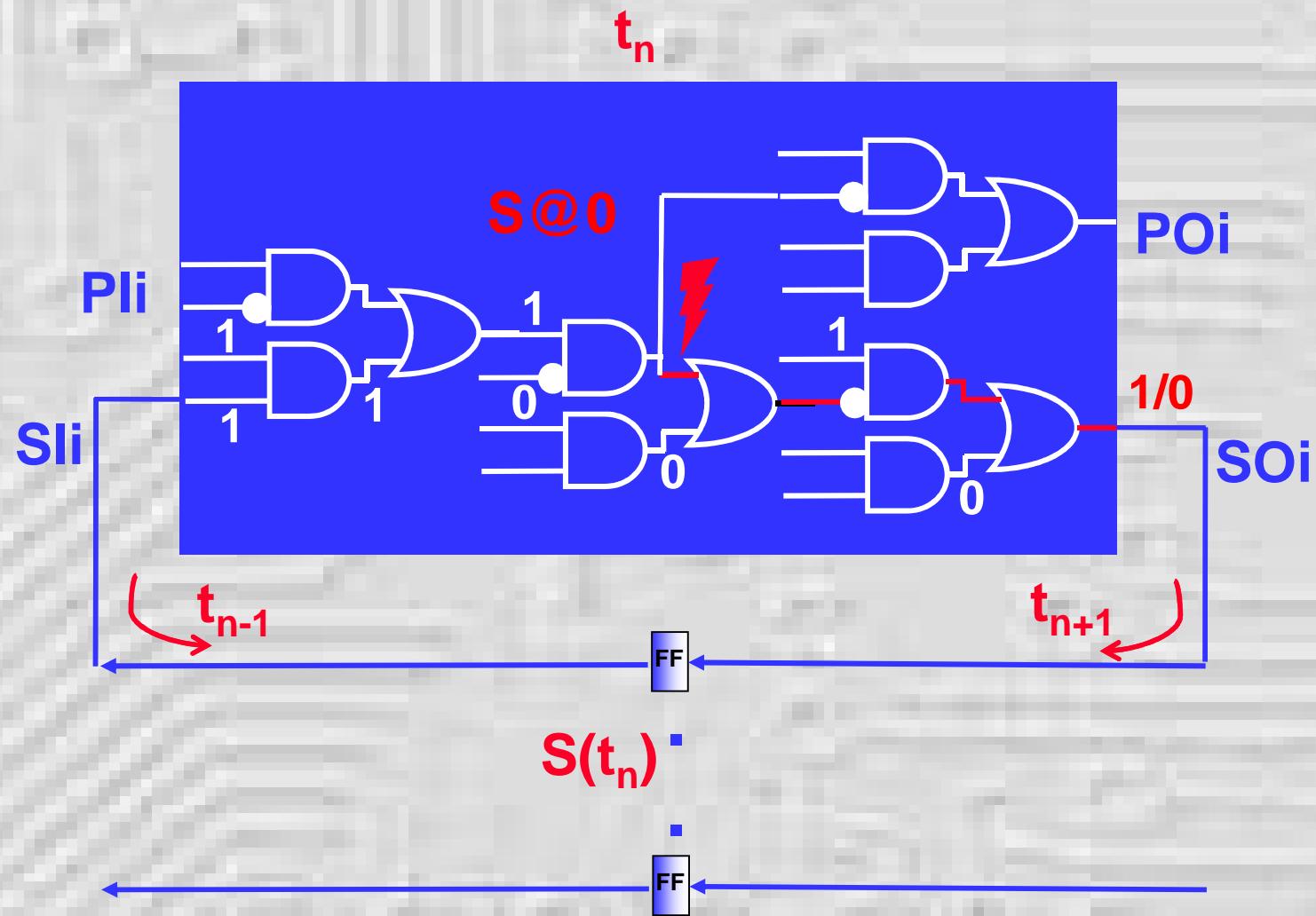


$$k=100$$

$$2^k=10^{31}$$

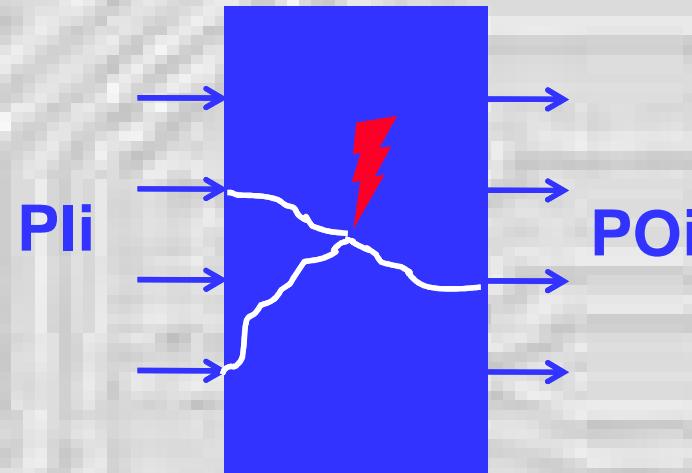


Sequential Logic

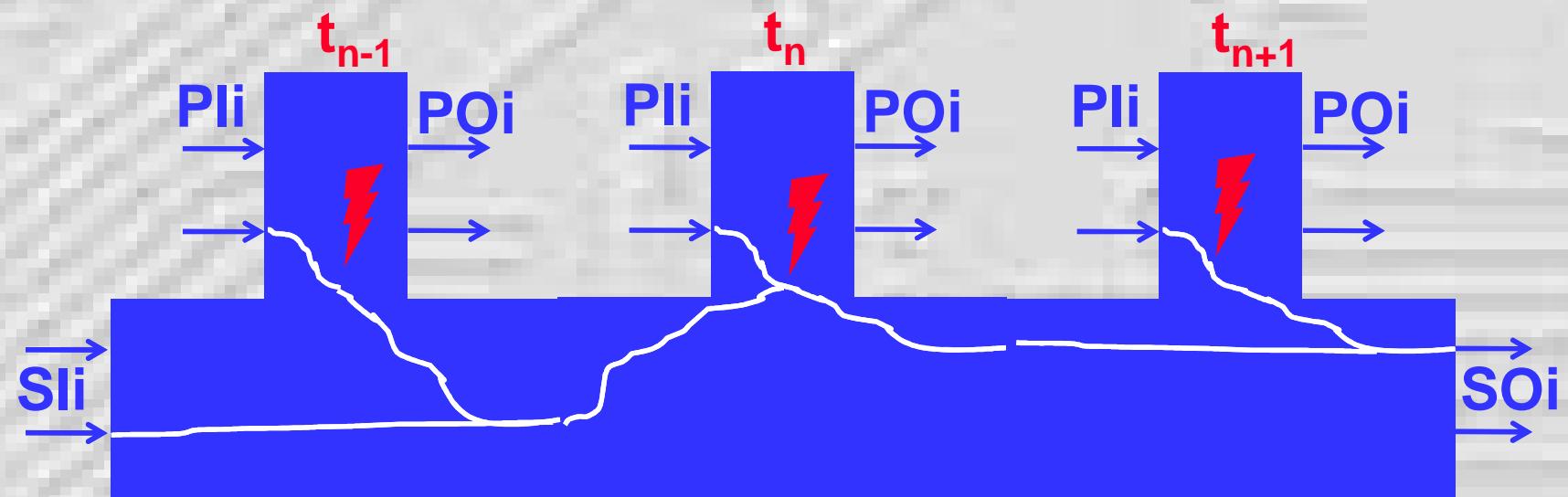


Structured DFT

IN2P3

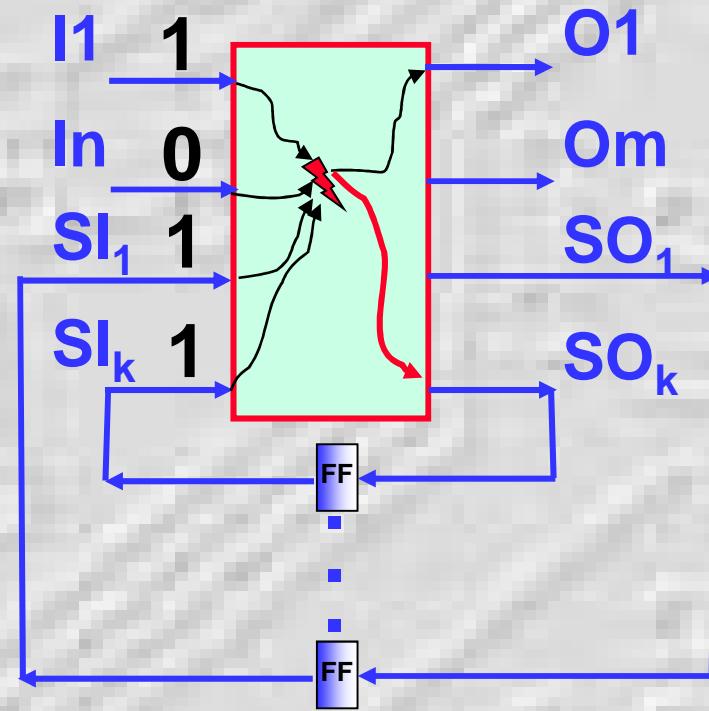


Sequential Logic

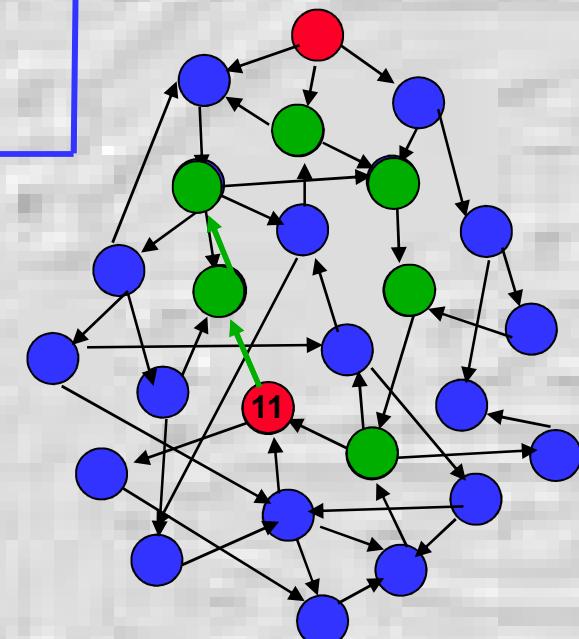


ATPG unfeasible

Structured DFT



$$L_{\text{seq}} = 10^7 \times L_{\text{comb}}$$



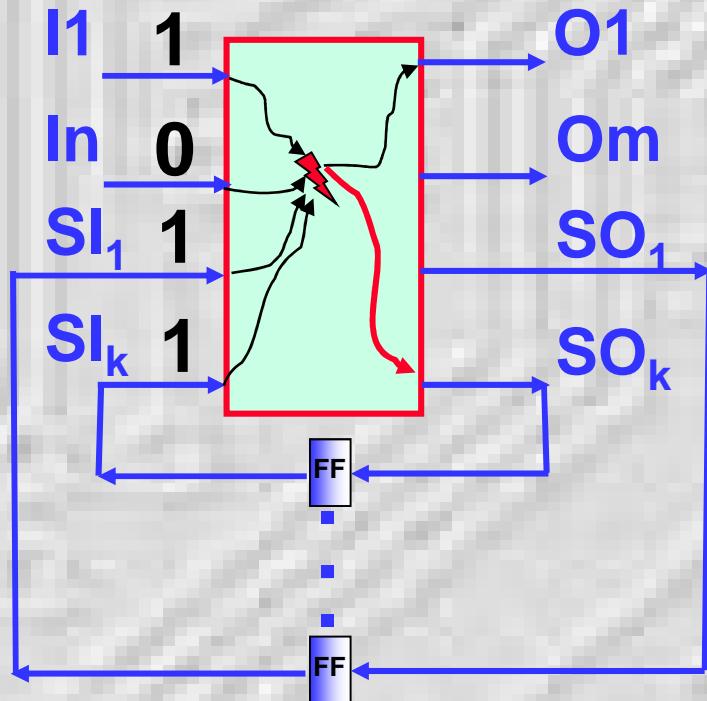
$$k=100$$

$$2^k = 10^{31}$$

$$N_T = 2^{k/4} \\ \sim 10^7$$

Structured DFT

IN2P3

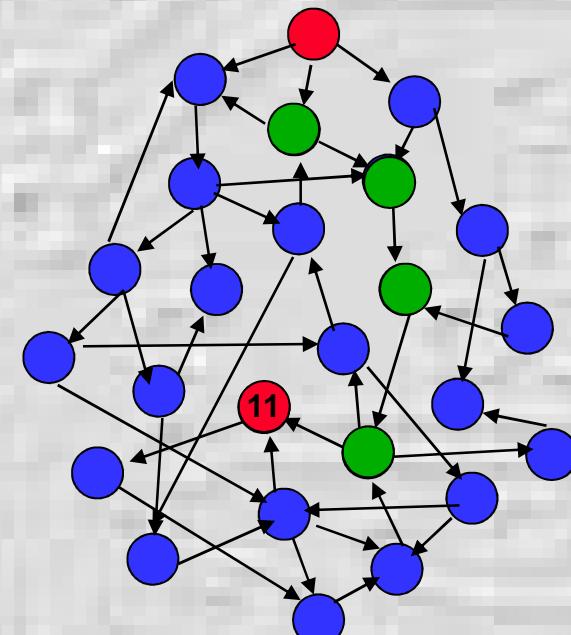


Combinational ATPG

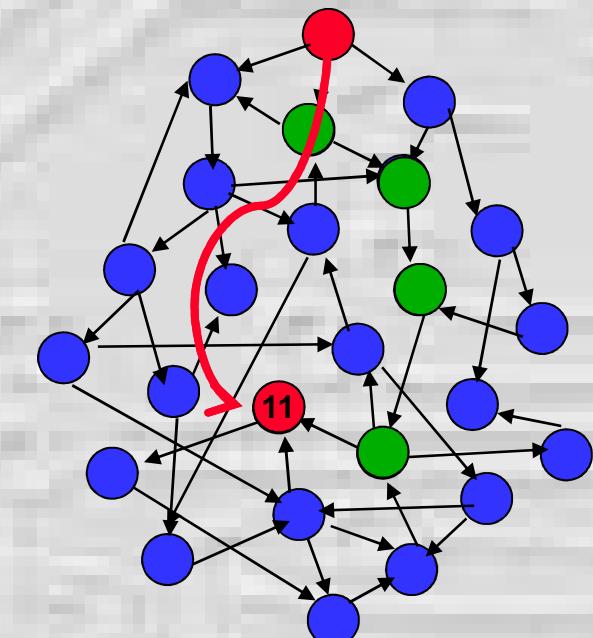
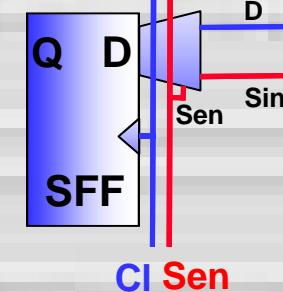
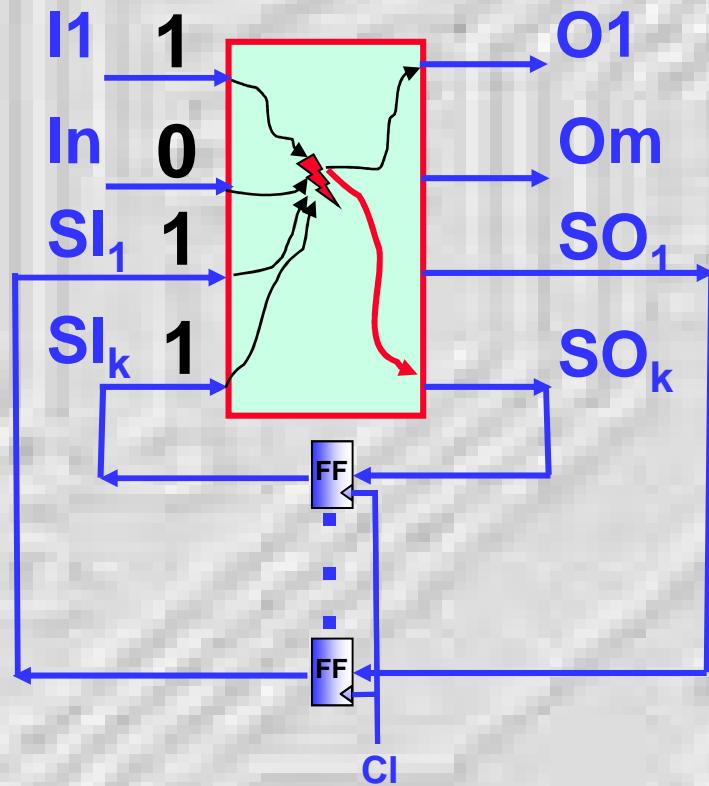
$$k=100$$

$$2^k = 10^{31}$$

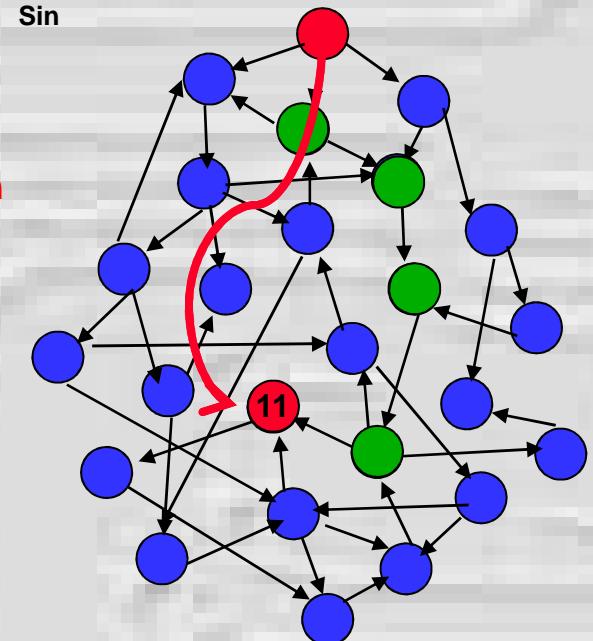
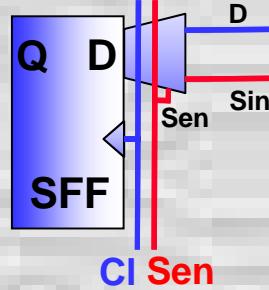
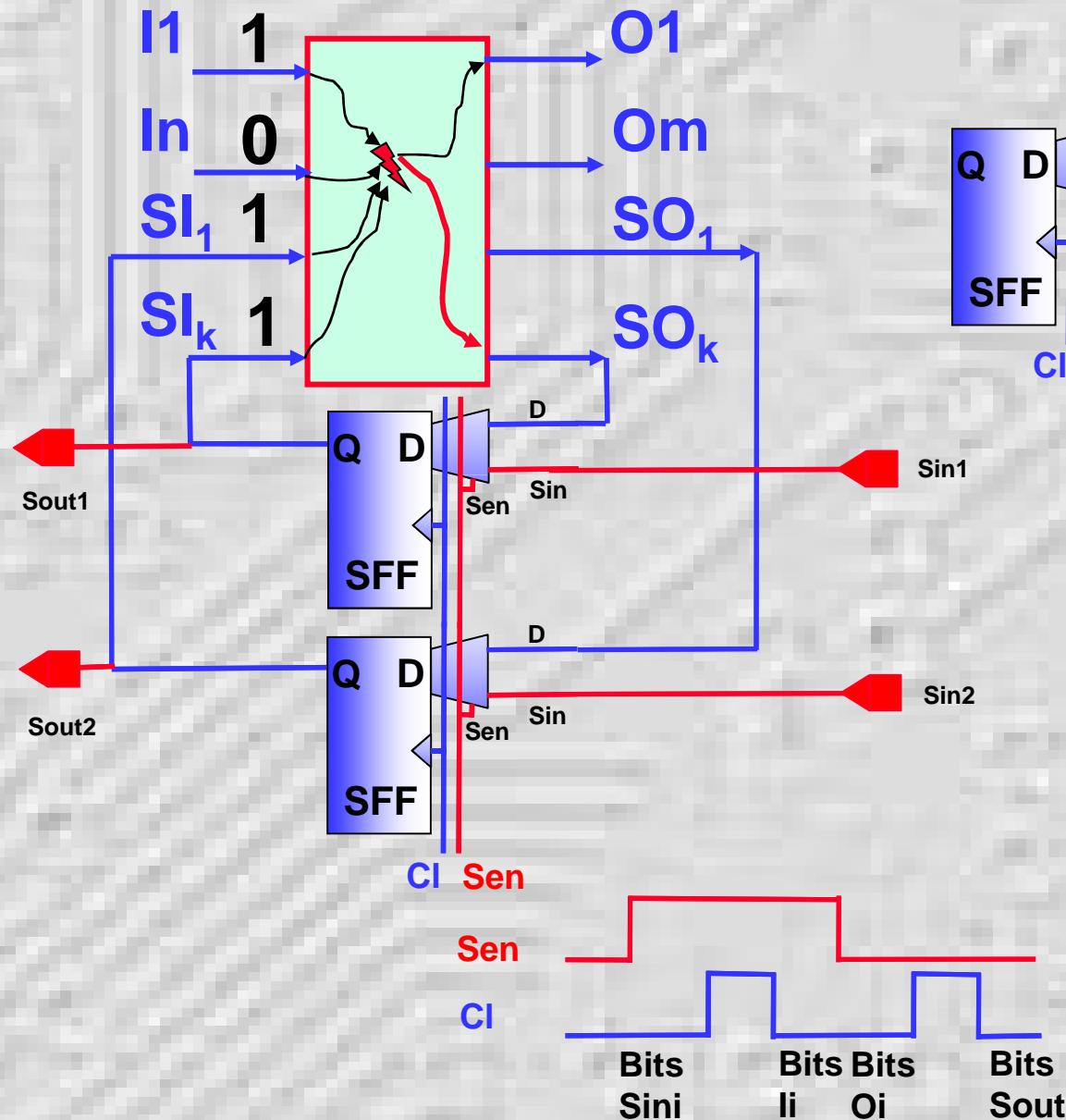
$$N_T = 2^{k/4} \sim 10^7$$



IN2P3



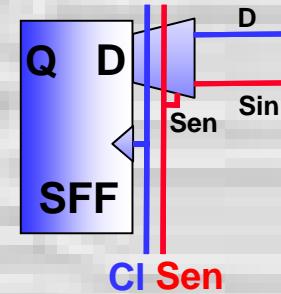
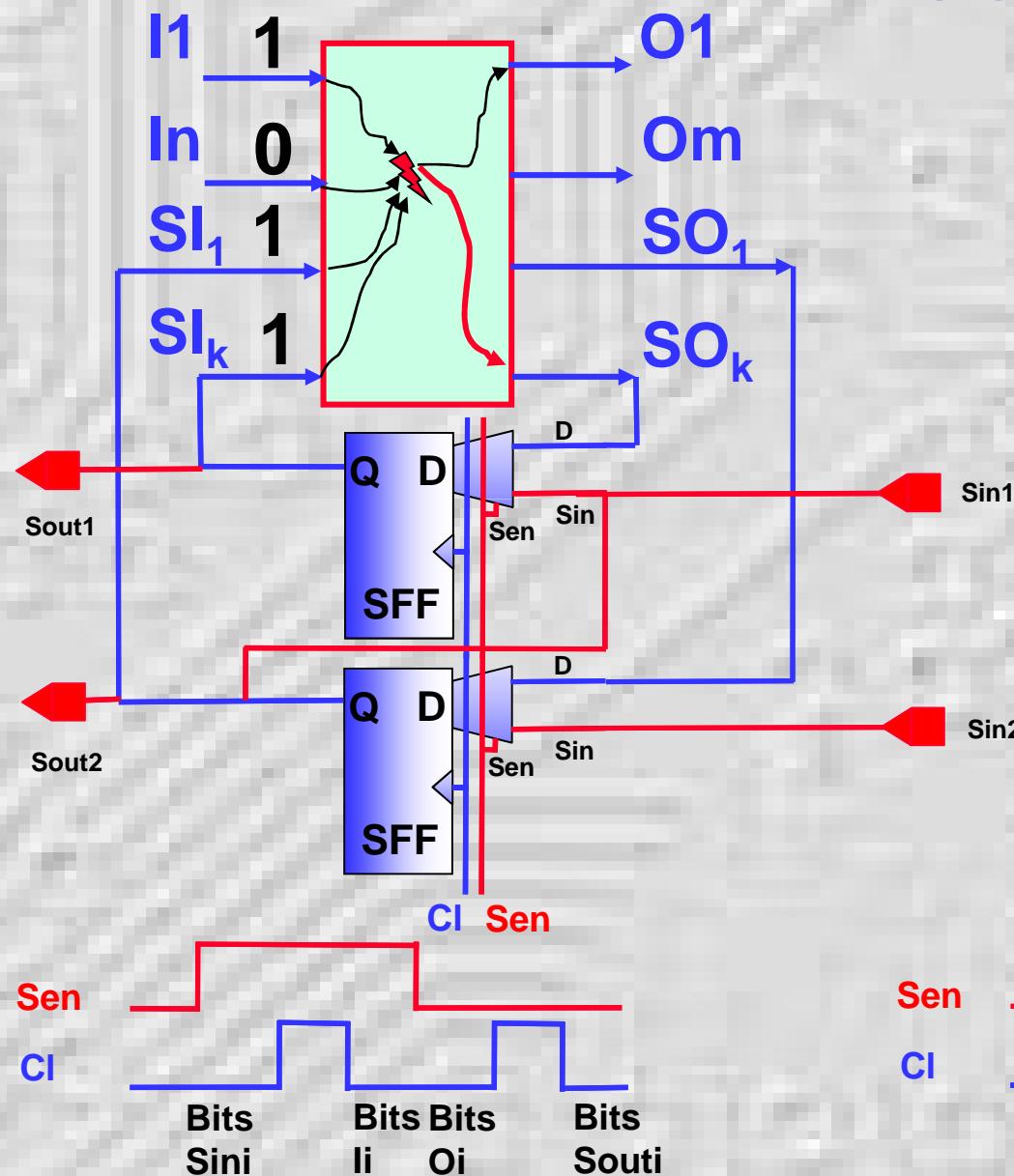
Structured DFT



- $L_{seq} = 2 \times L_{comb}$
- $N_{pin} = 2k+1$

IN2P3

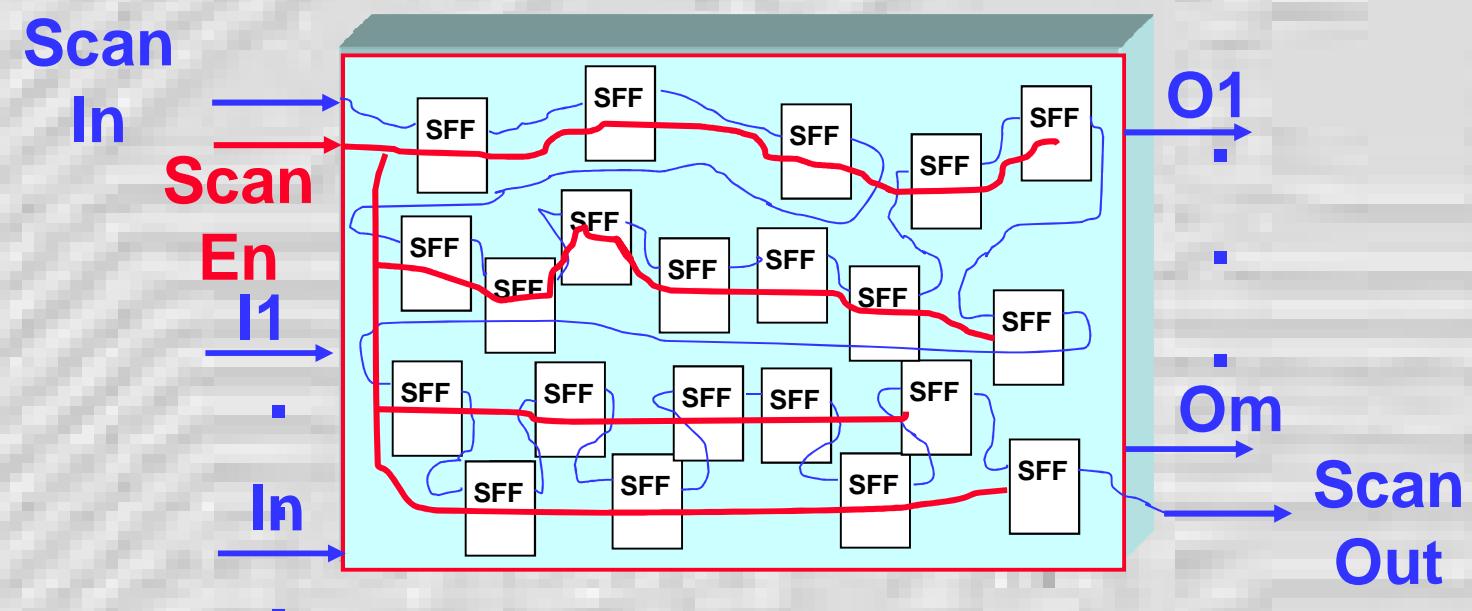
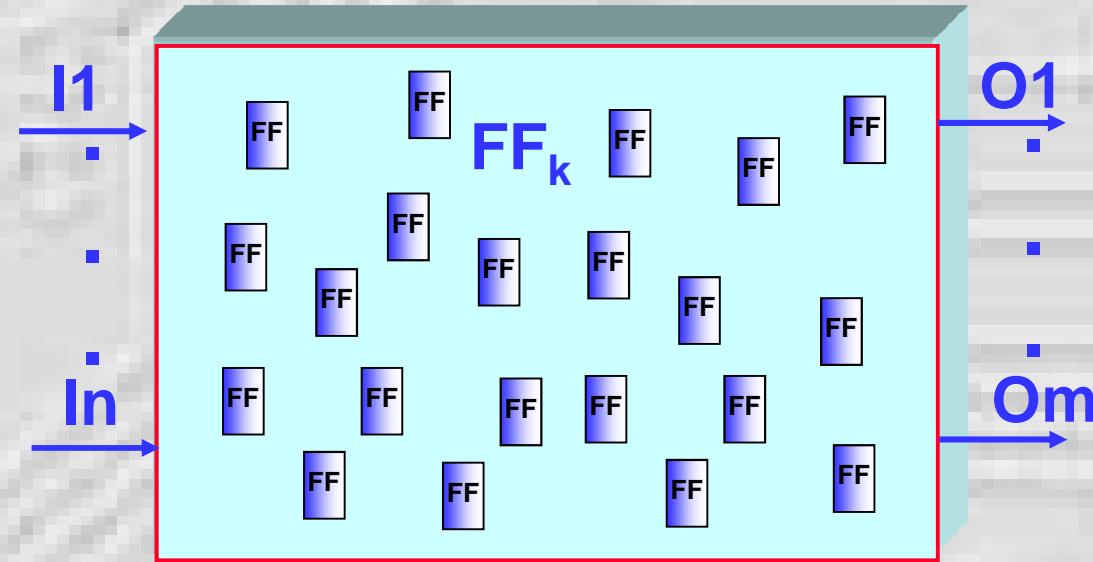
SCAN Design

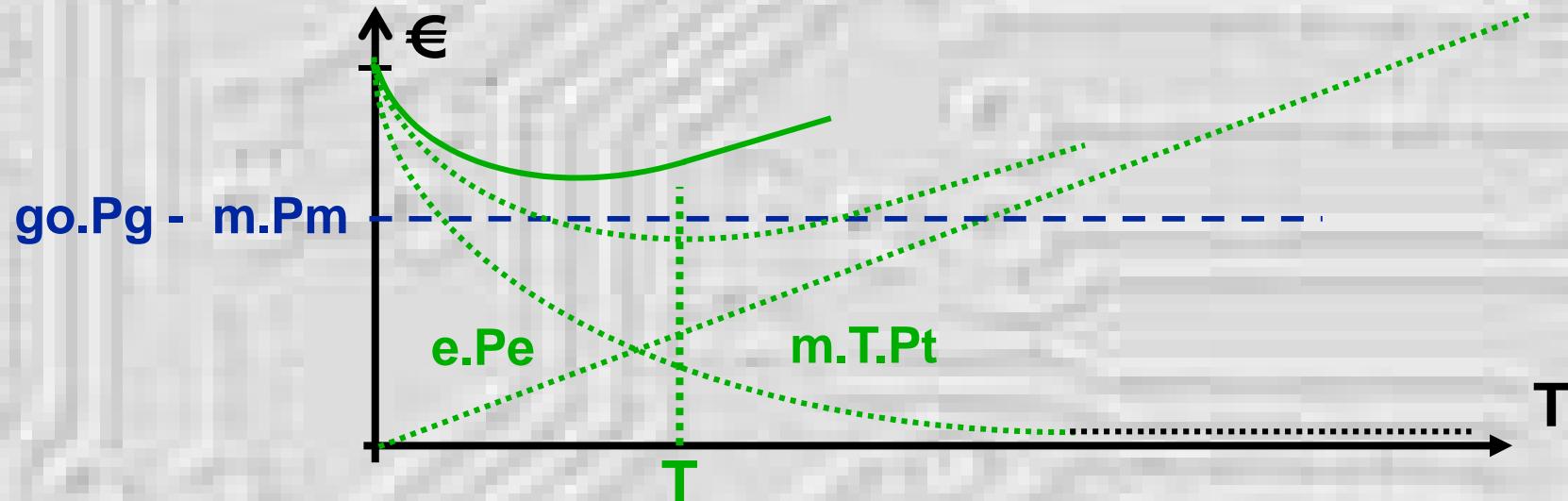


- $L_{seq} = k \times L_{comb}$
 - $N_{pin} = 2+1$

Structured DFT Sequential Logic

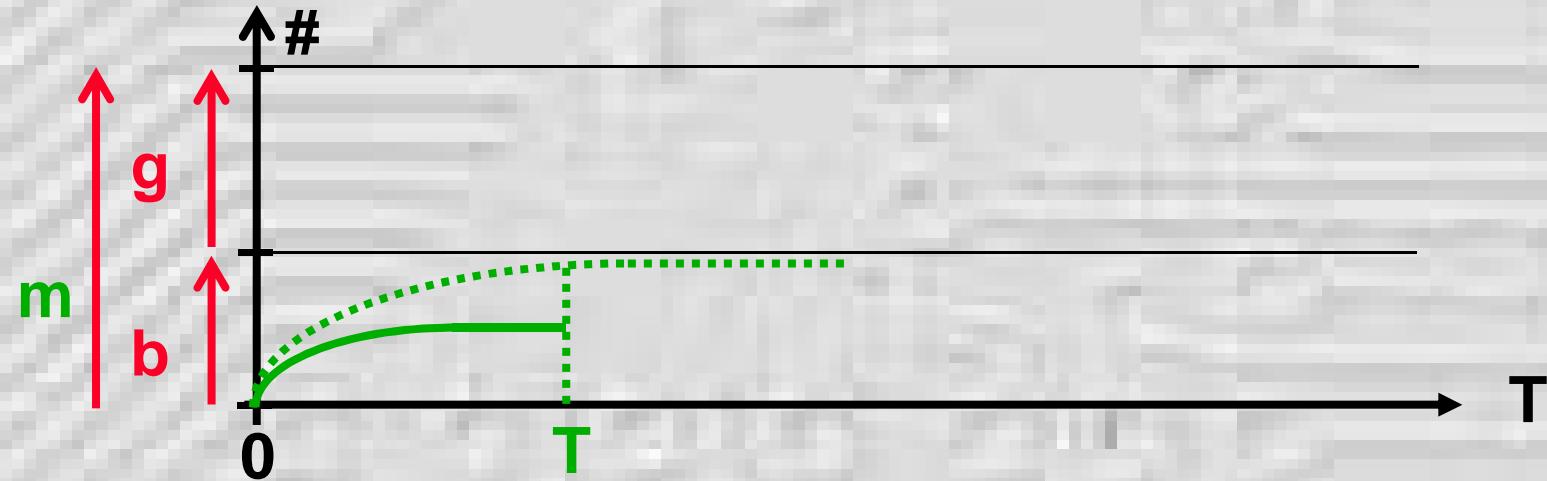
IN2P3

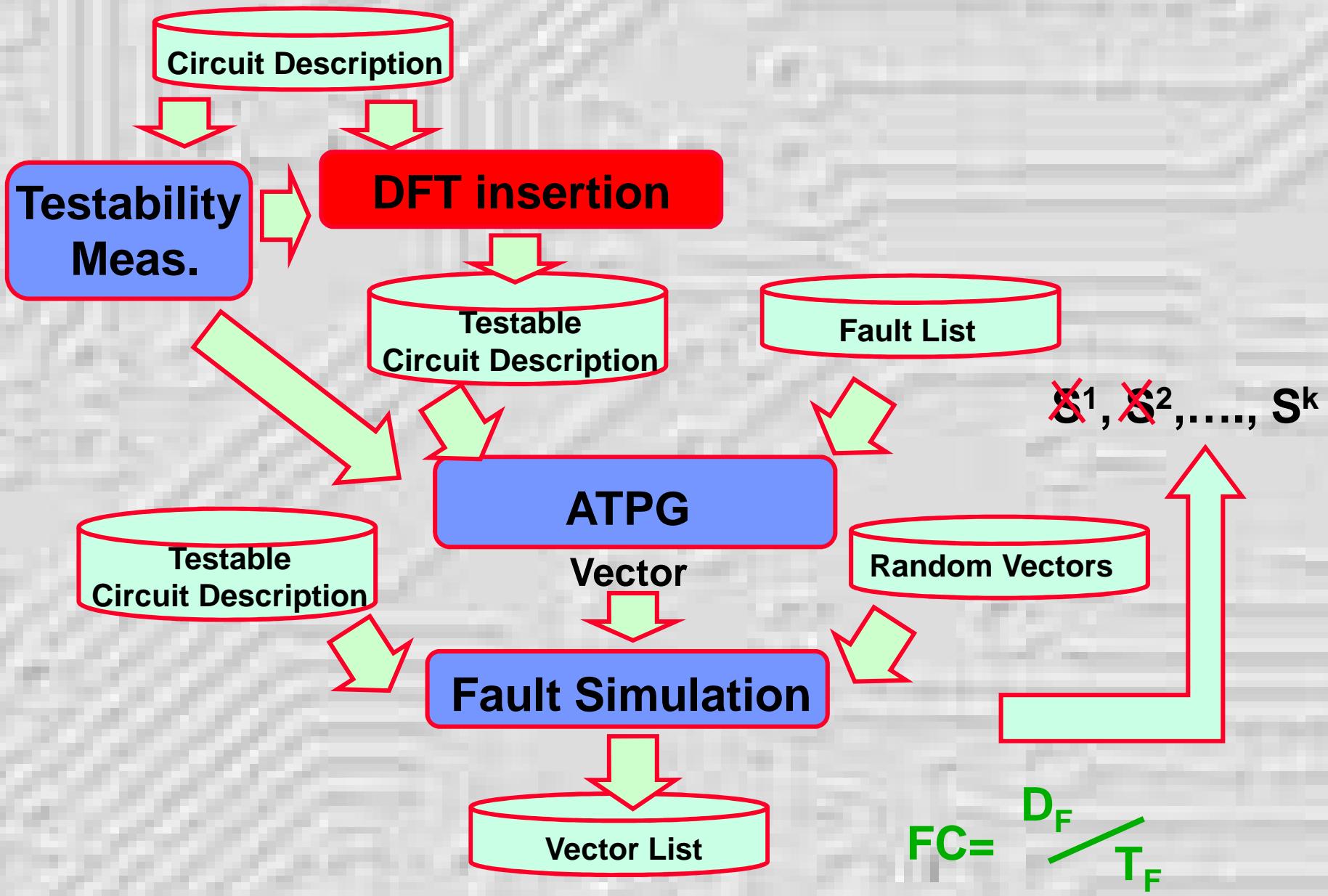




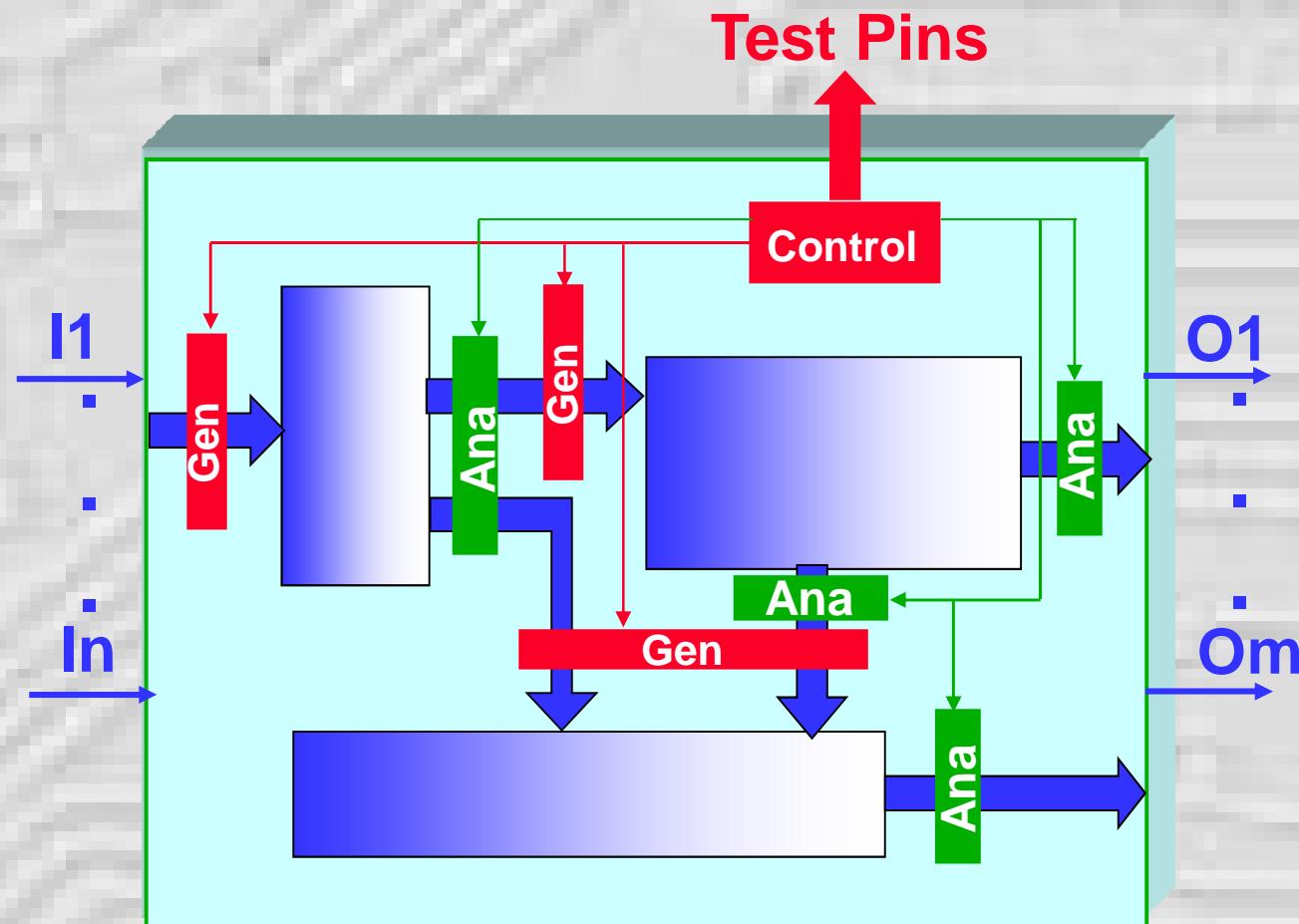
III) Criteria to make circuit Testable

=> Propose circuit modifications



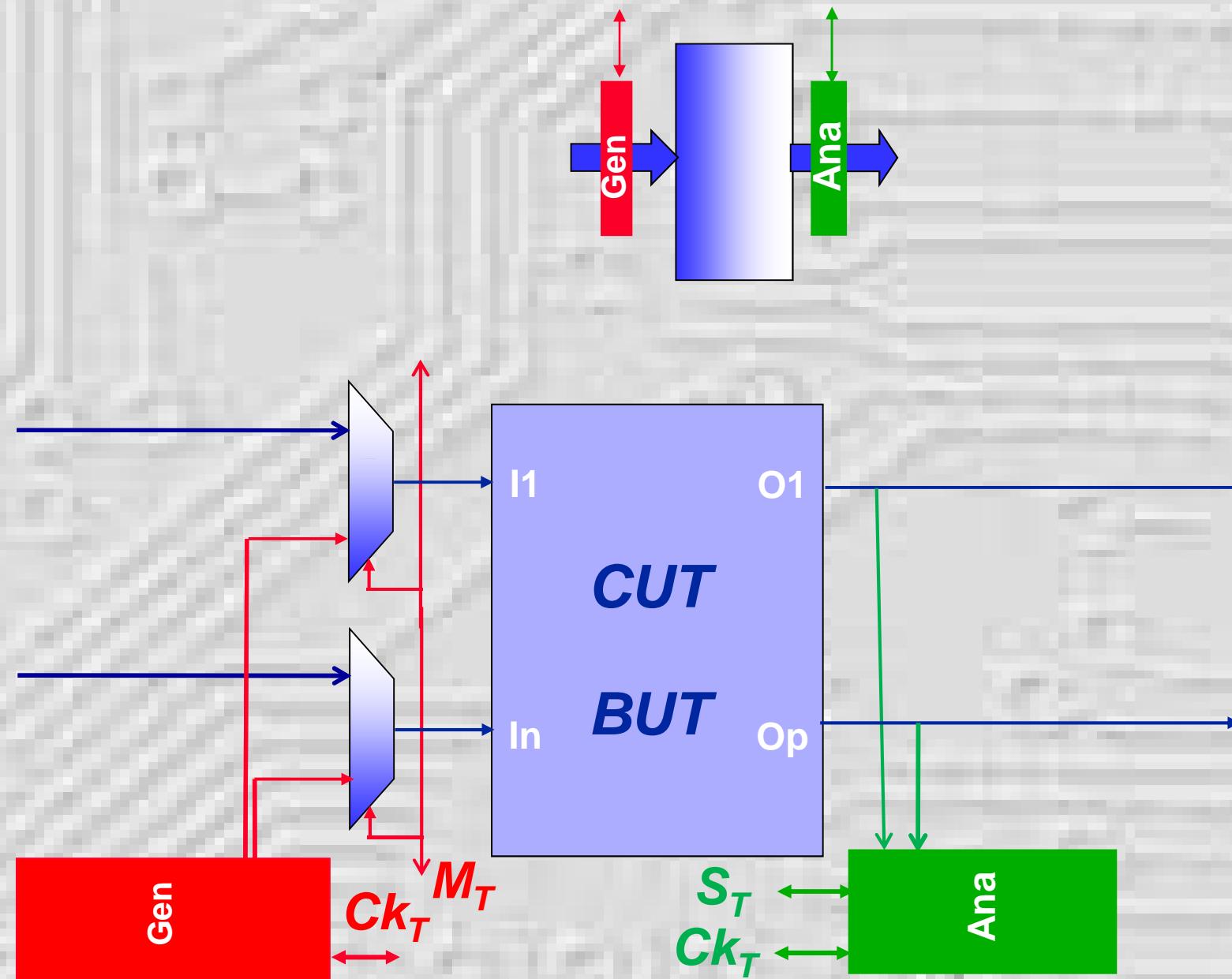


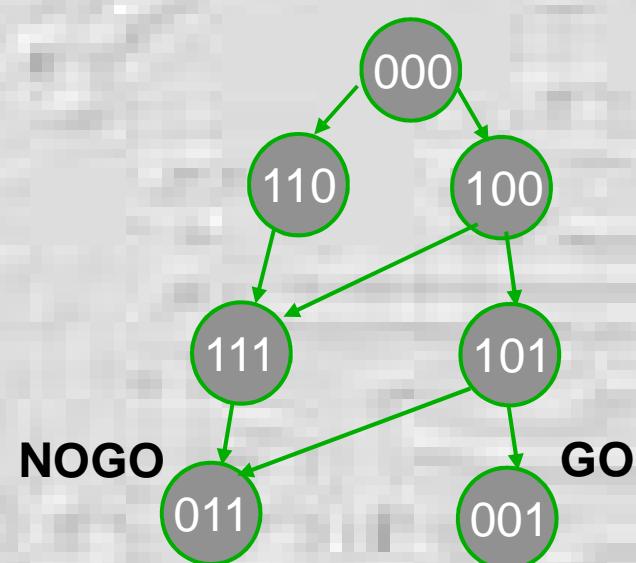
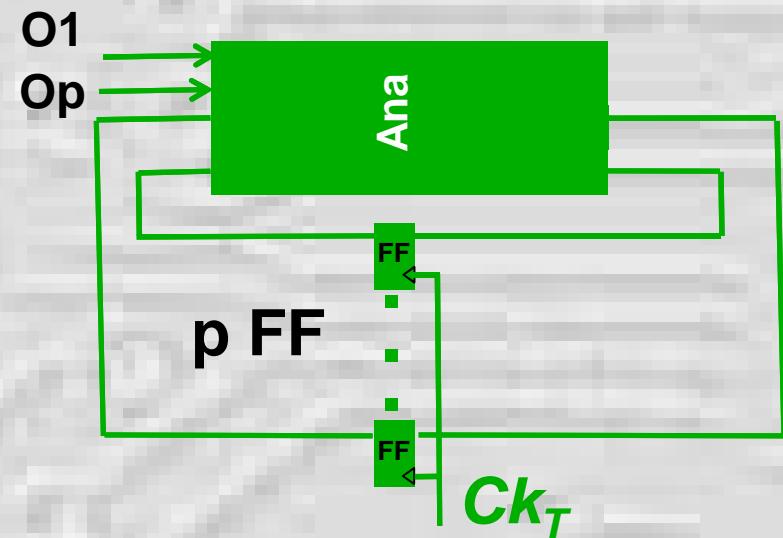
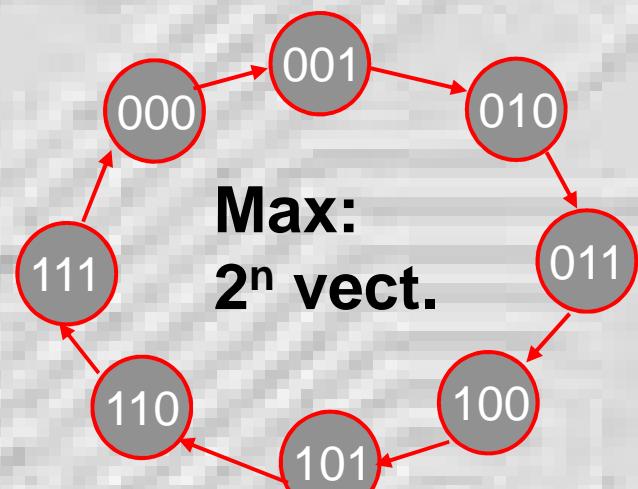
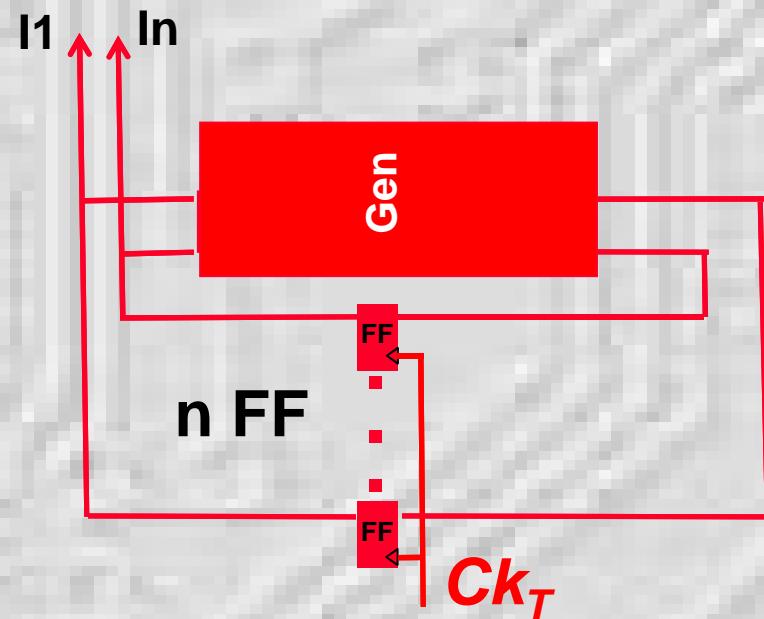
Built -In Self-Test



BIST

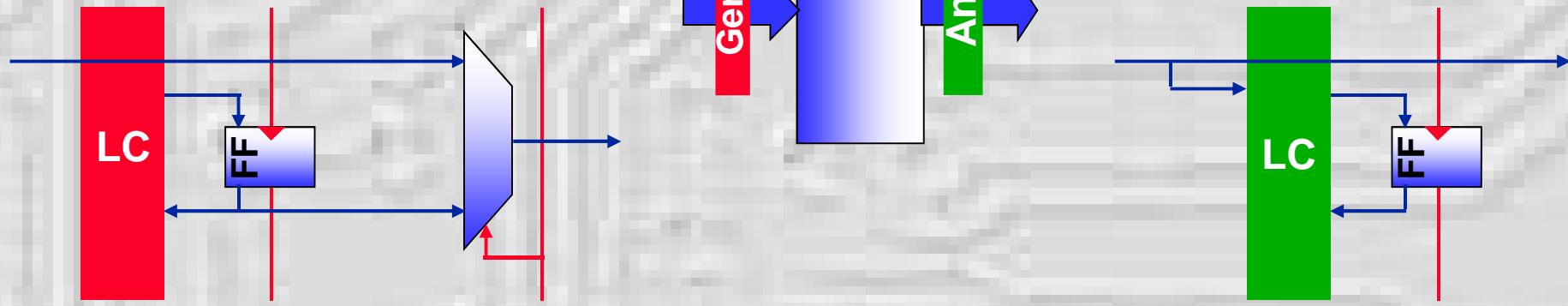
IN2P3





BIST

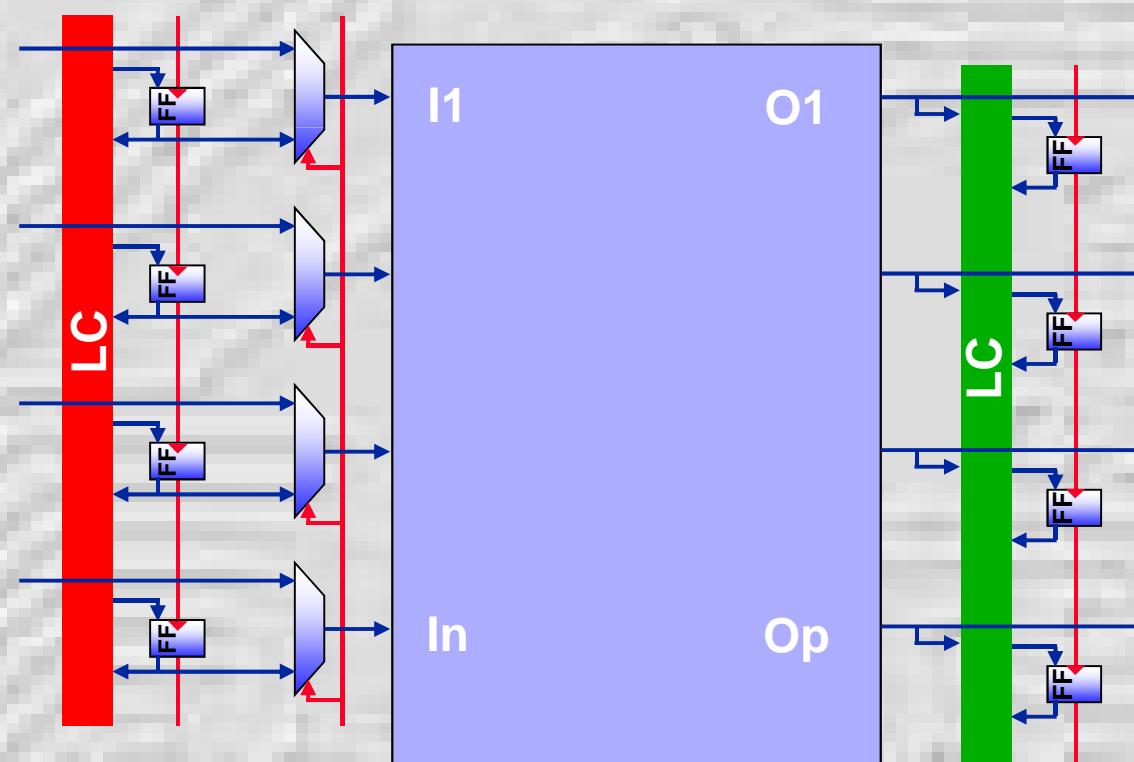
IN2P3

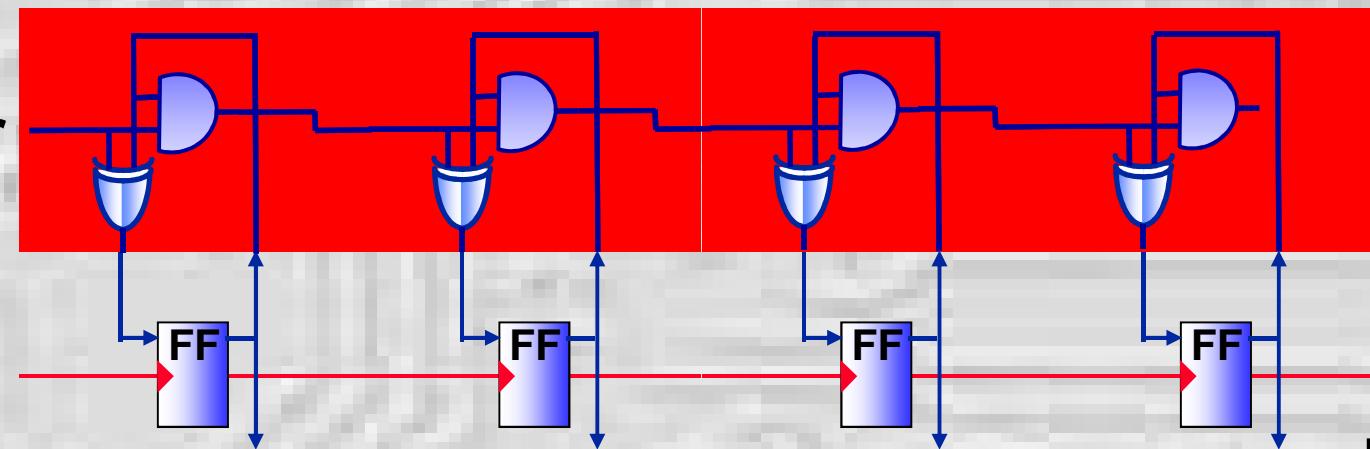
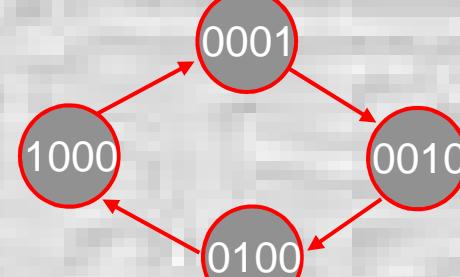
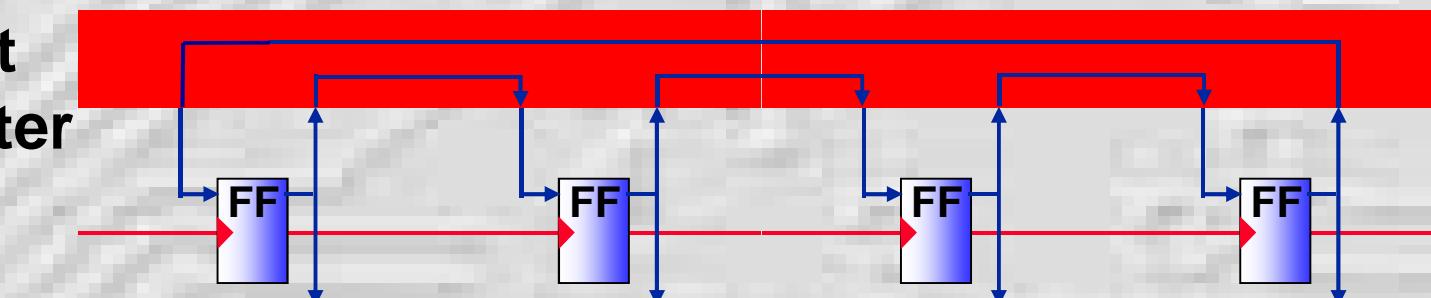


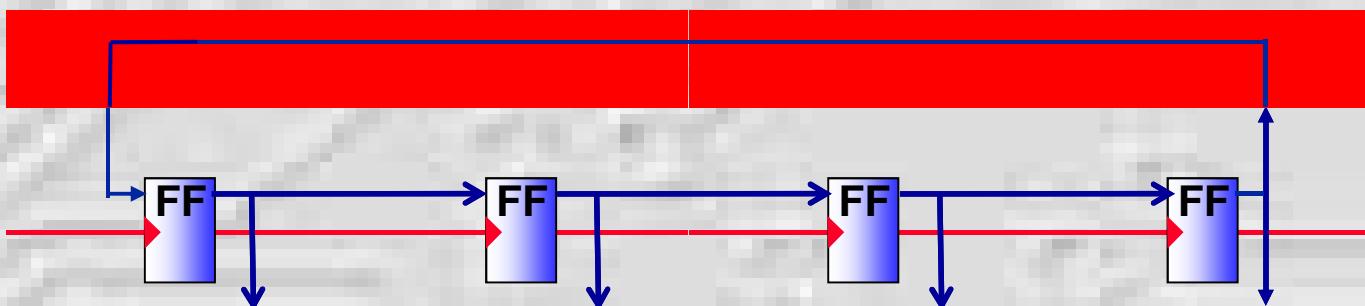
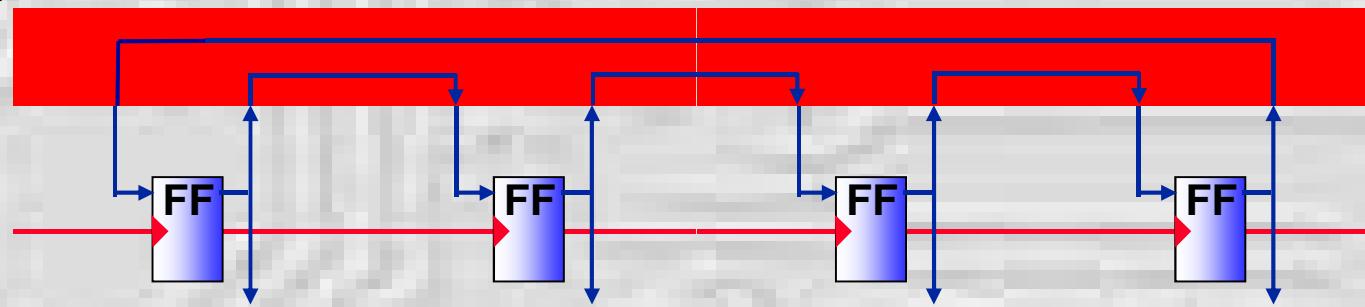
n FF

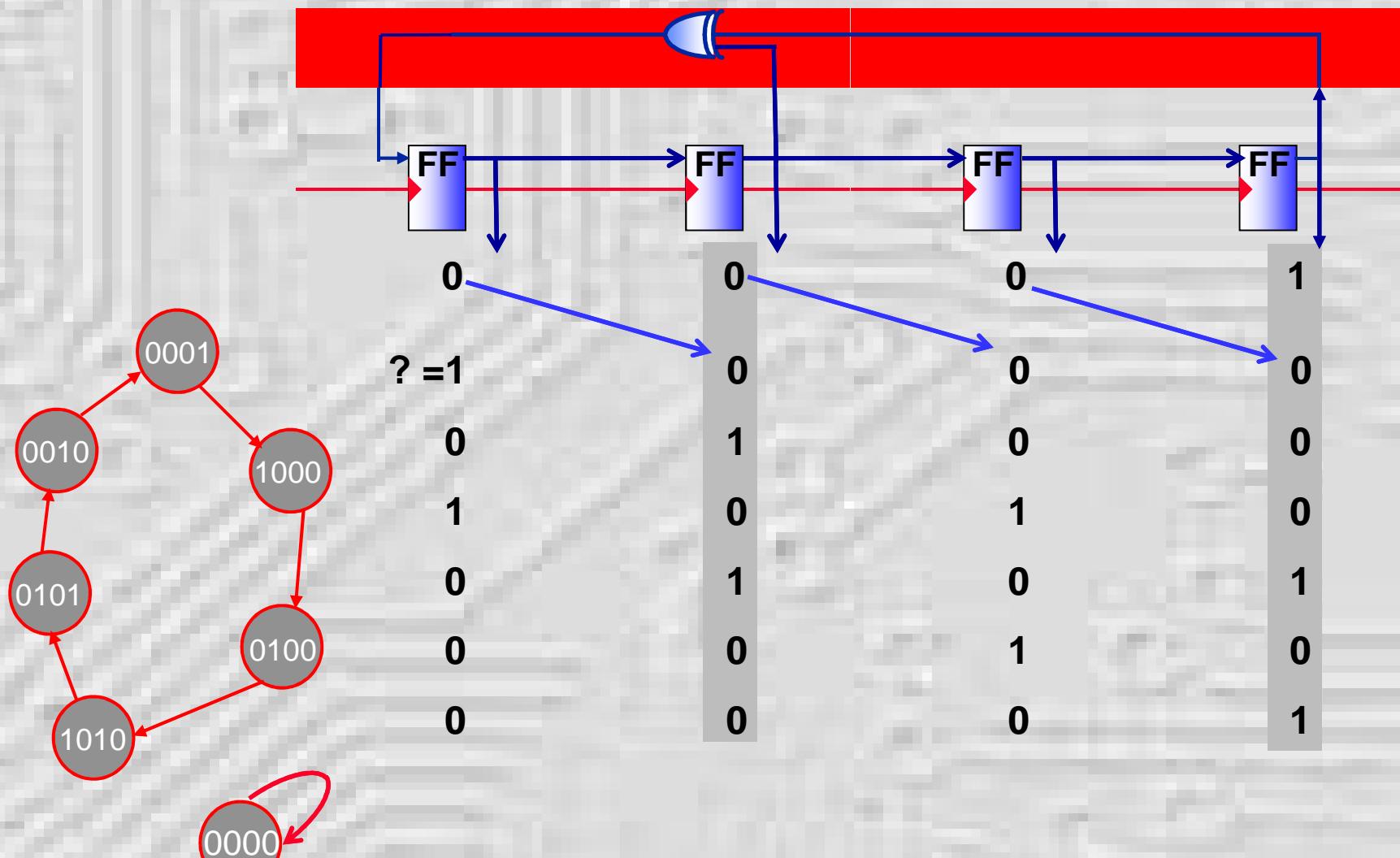
Max:

2^n vect.

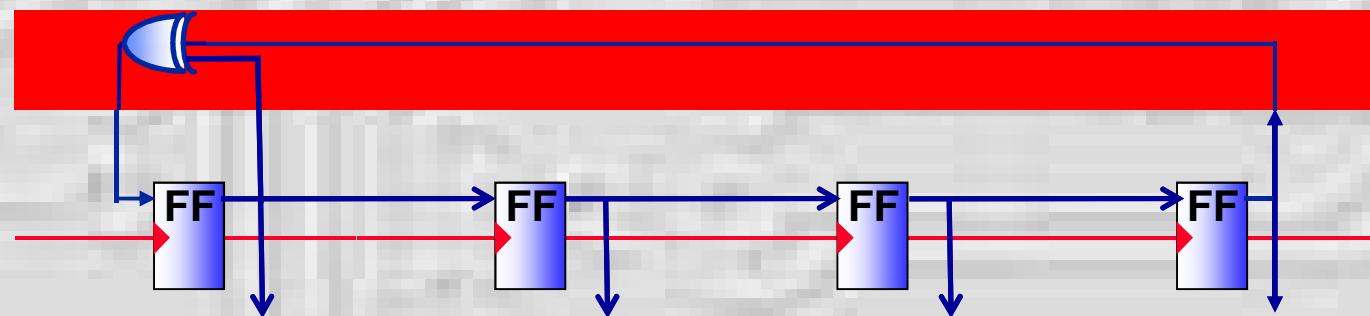


Counter**Feedback Shift Register**

Feedback Shift Register



LFSR = Linear Feedback Shift Register



$2^4 - 1$
Vectors !

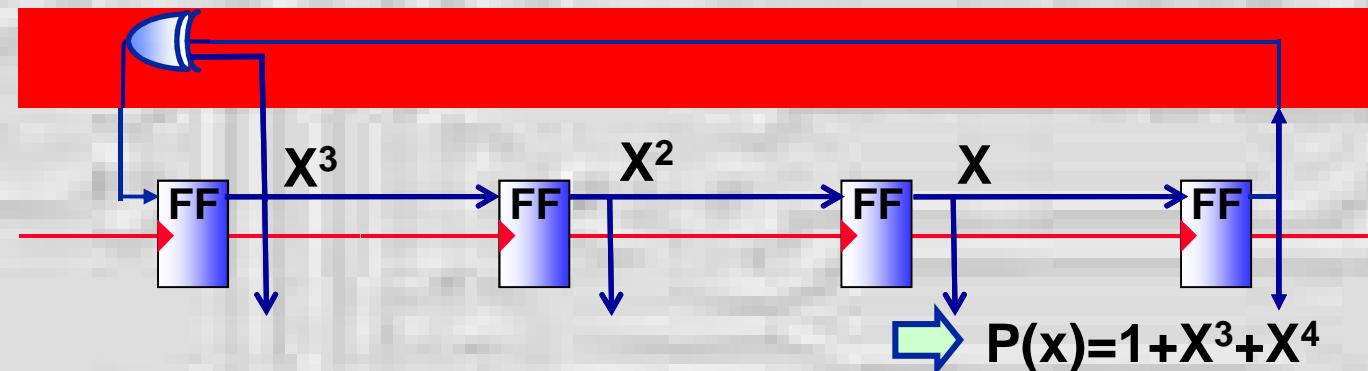
$\begin{bmatrix} 0 \\ 1 \\ 1 \\ 1 \\ 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 1 \\ 1 \\ 0 \\ 0 \\ 1 \\ 0 \\ 0 \end{bmatrix}$

$\begin{bmatrix} 0 \\ 0 \\ 1 \\ 1 \\ 1 \\ 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 0 \\ 0 \\ 1 \\ 0 \\ 0 \end{bmatrix}$

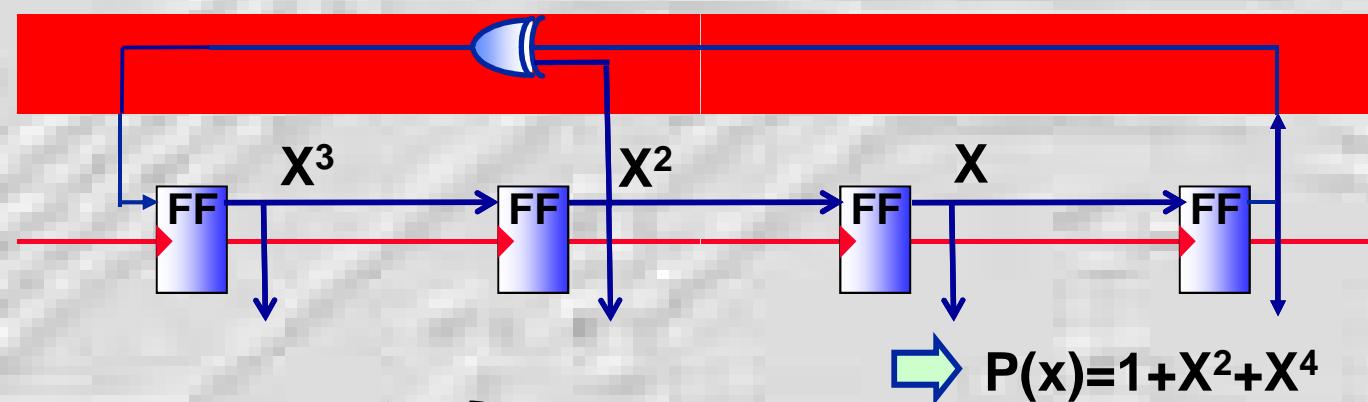
$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \\ 1 \\ 1 \\ 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 1 \\ 0 \\ 0 \\ 1 \end{bmatrix}$

$\begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 1 \\ 1 \\ 1 \\ 1 \\ 0 \\ 1 \\ 1 \\ 0 \\ 1 \\ 0 \\ 0 \\ 1 \end{bmatrix}$

LFSR2
15 vect.



LFSR1
6 vect.



$$P(X) = \sum X_i \text{ with } X \in B = [0, 1]$$

XOR, AND

Galois Field

Primitive $P(x)$ $\rightarrow 2^n - 1$

$$\begin{array}{r}
 X^4 + X^2 + 1 \\
 X^4 + X^3 + X^2 \\
 \hline
 X^3 + 1 \\
 X^3 + X^2 + X \\
 \hline
 X^2 + X + 1 \\
 X^2 + X + 1 \\
 \hline
 0
 \end{array}$$

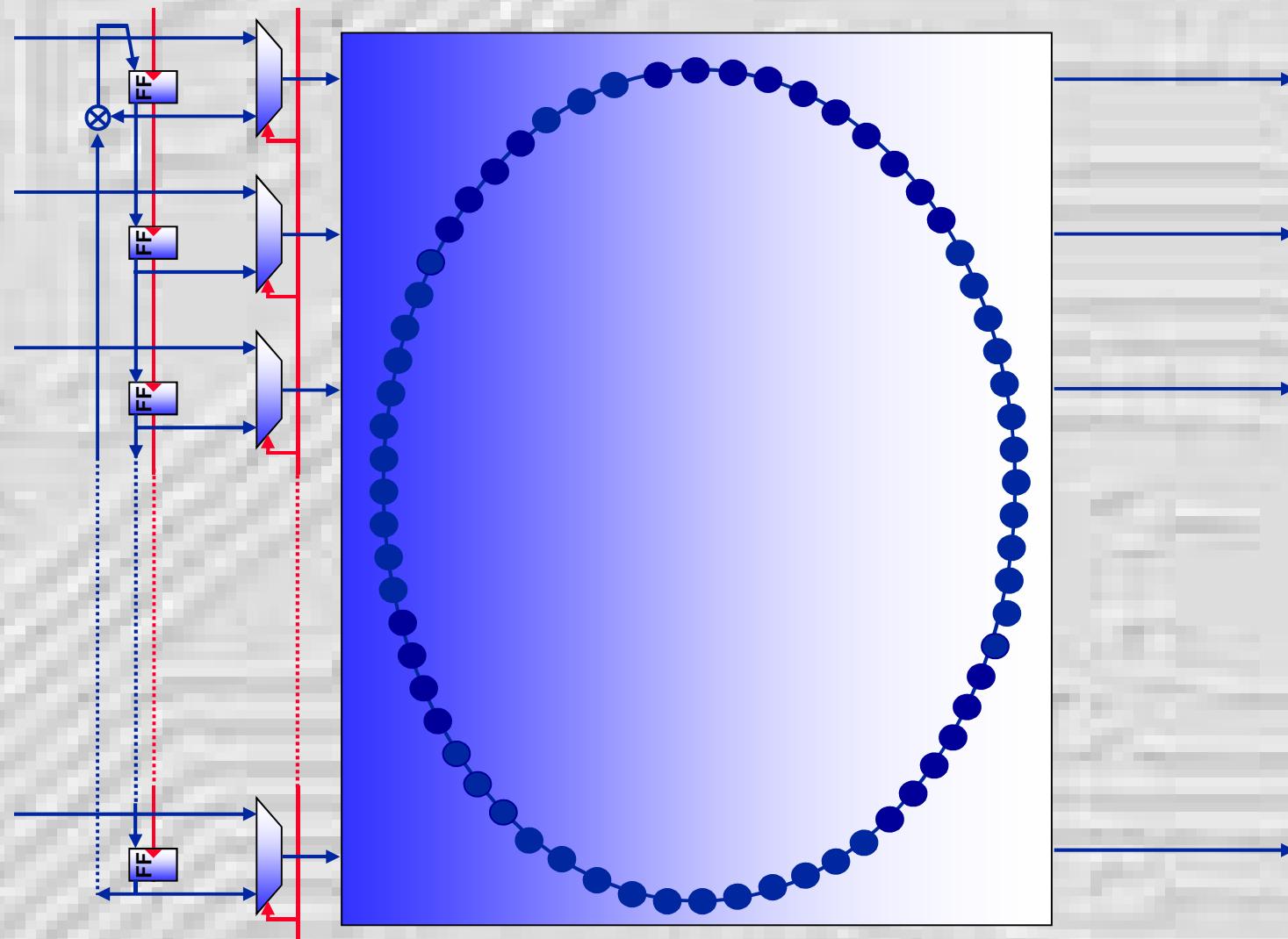
degré						degré						degré					
1	0					13	4	3	1	0		25	3	0			
2	1	0				14	12	11	1	0		26	8	7	1	0	
3	1	0				15	1	0				27	8	7	1	0	
4	1	0				16	5	3	2	0		28	3	0			
5	2	0				17	3	0				29	2	0			
6	1	0				18	7	0				30	16	15	1	0	
7	1	0				19	6	5	1	0		31	3	0			
8	6	5	1	0		20	3	0				32	28	27	1	0	
9	4	0				21	2	0				33	13	0			
10	3	0				22	1	0				34	15	14	1	0	
11	2	0				23	5	0				35	2	0			
12	7	4		0		24	4	3	1	0		36	11	0			

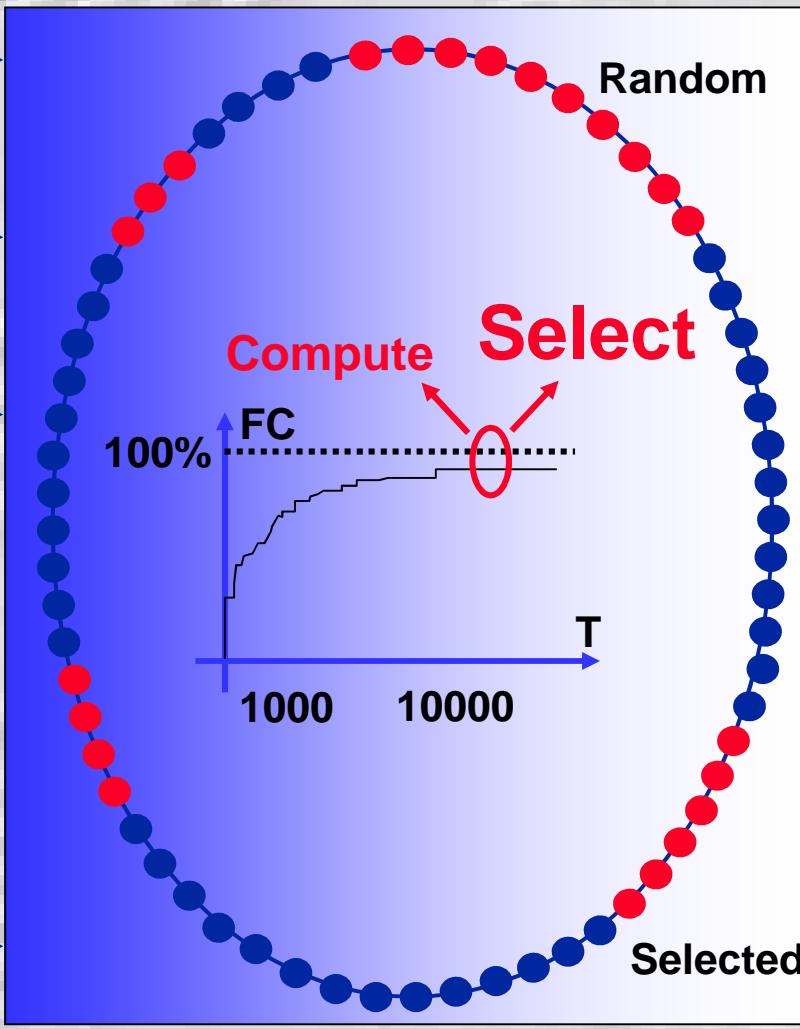
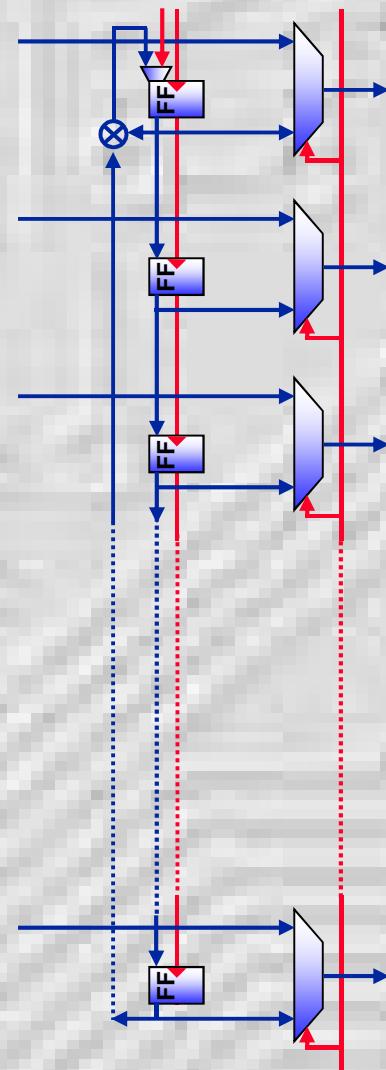
$$P(x) = x^{34} + x^{15} + x^{14} + x + 1$$

$$P(x) = x^{22} + x + 1$$

BIST

IN2P3





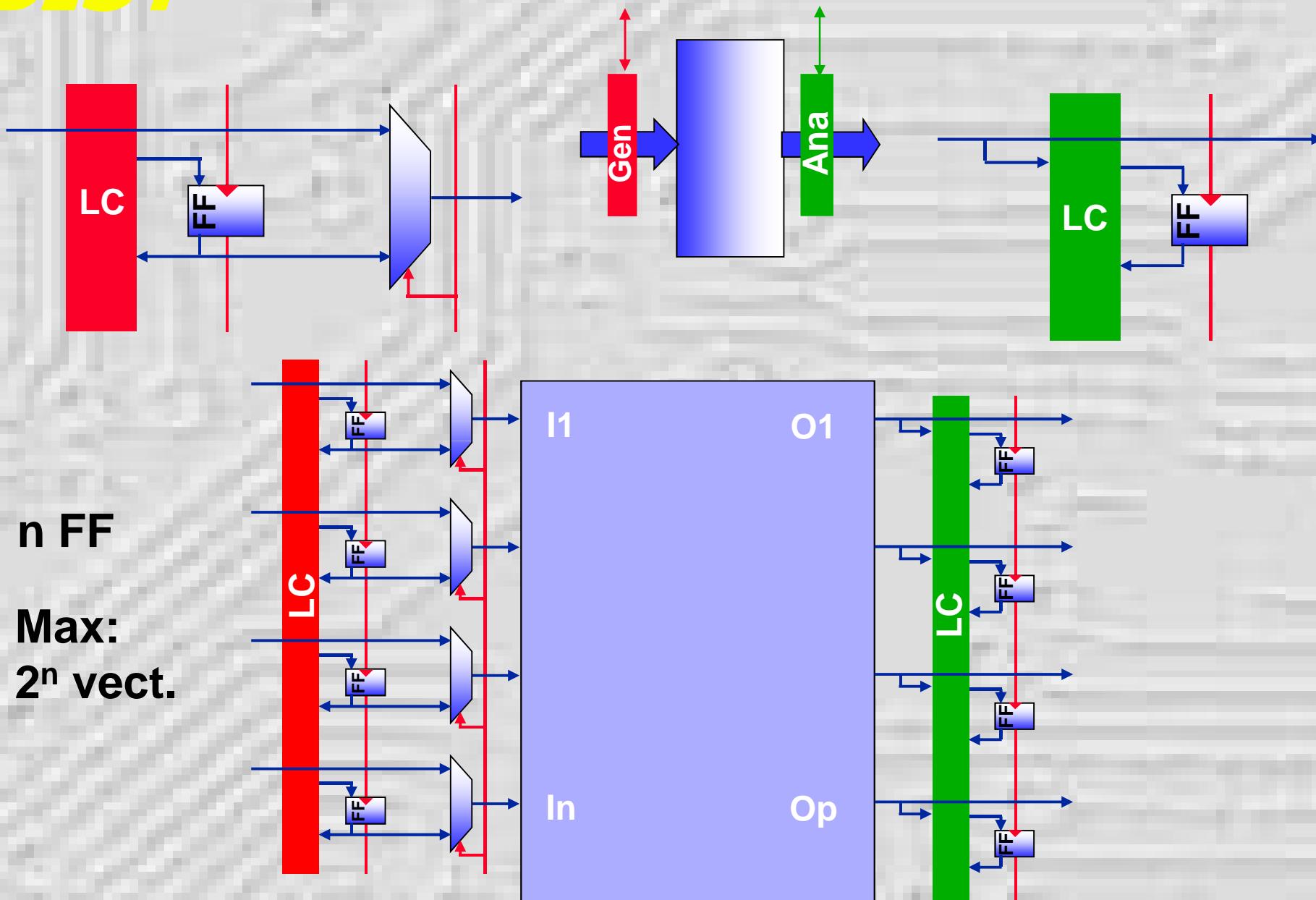
■ Test Length²

■ Seed/Clock

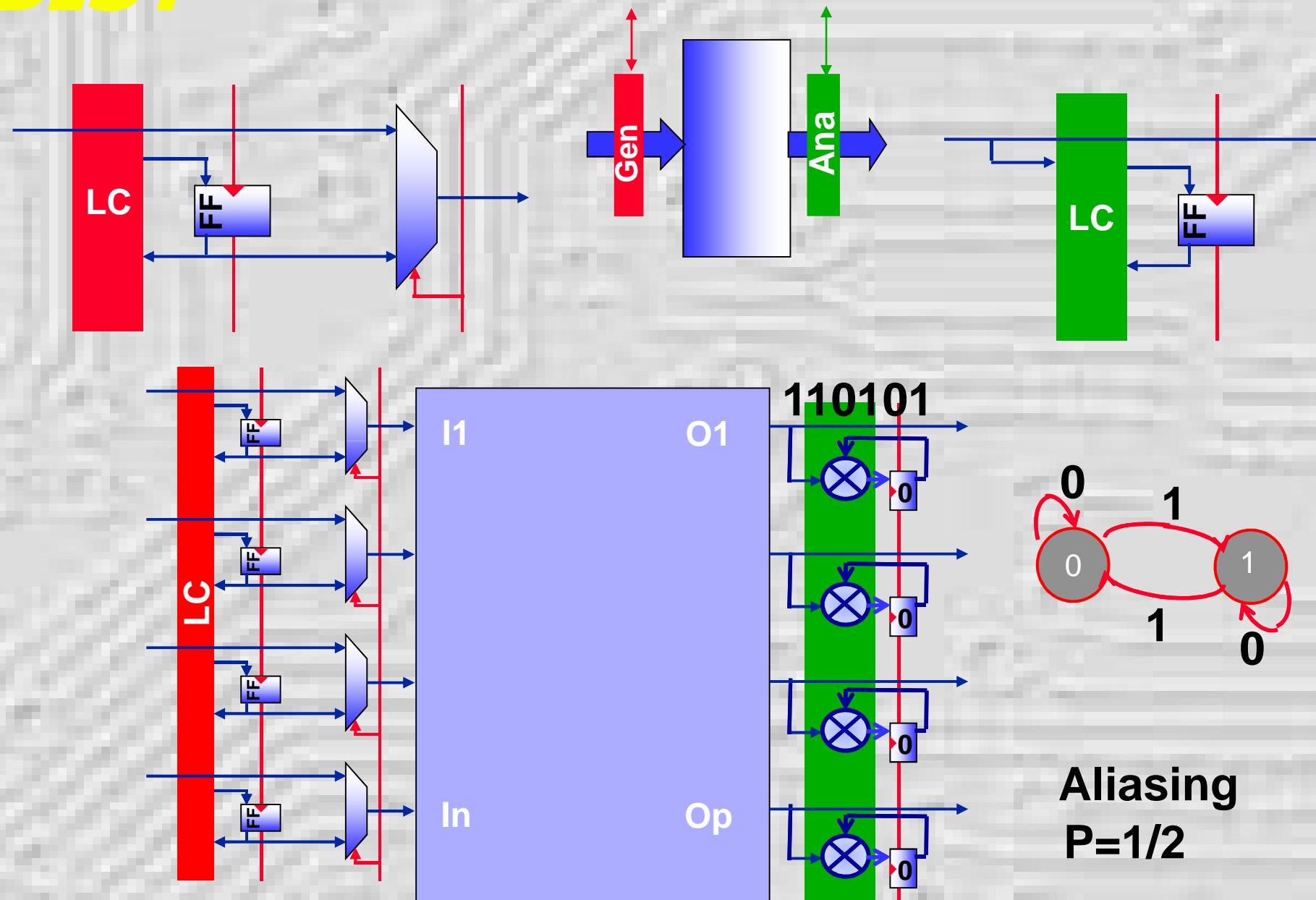
■ Reconf Polyn

BIST

IN2P3

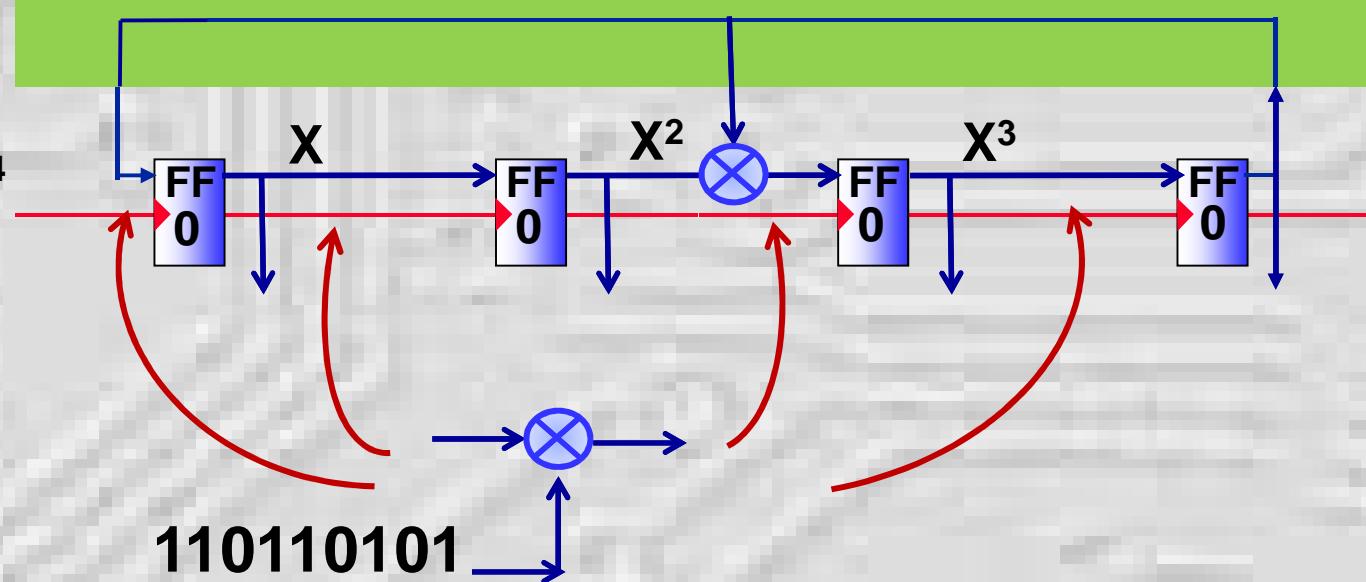


IN2P3

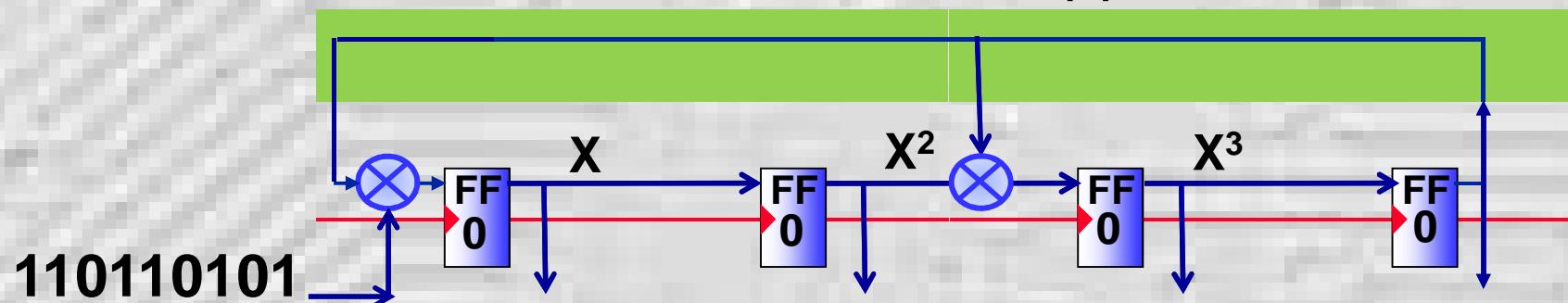


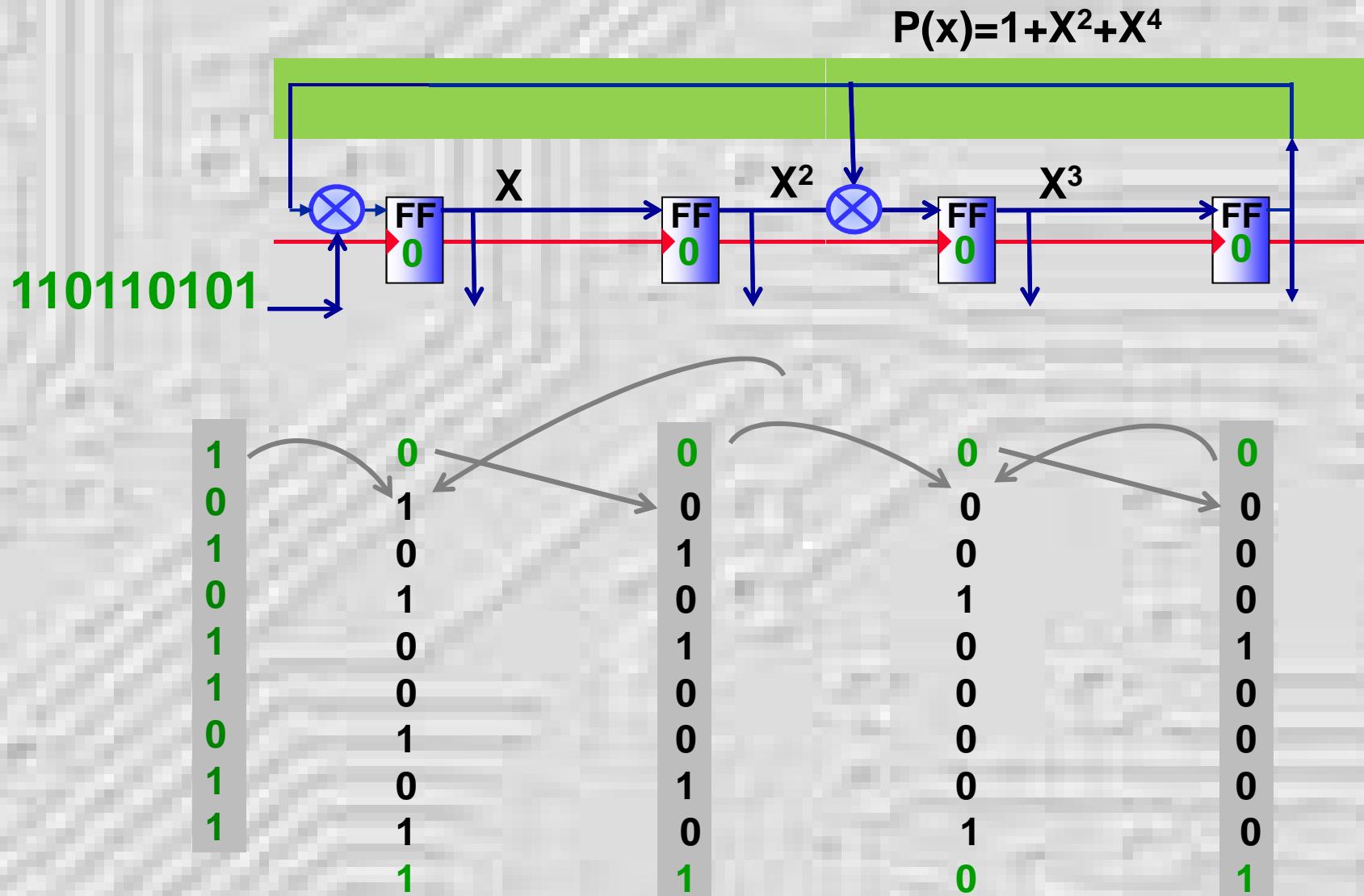
**Internal
LFSR**

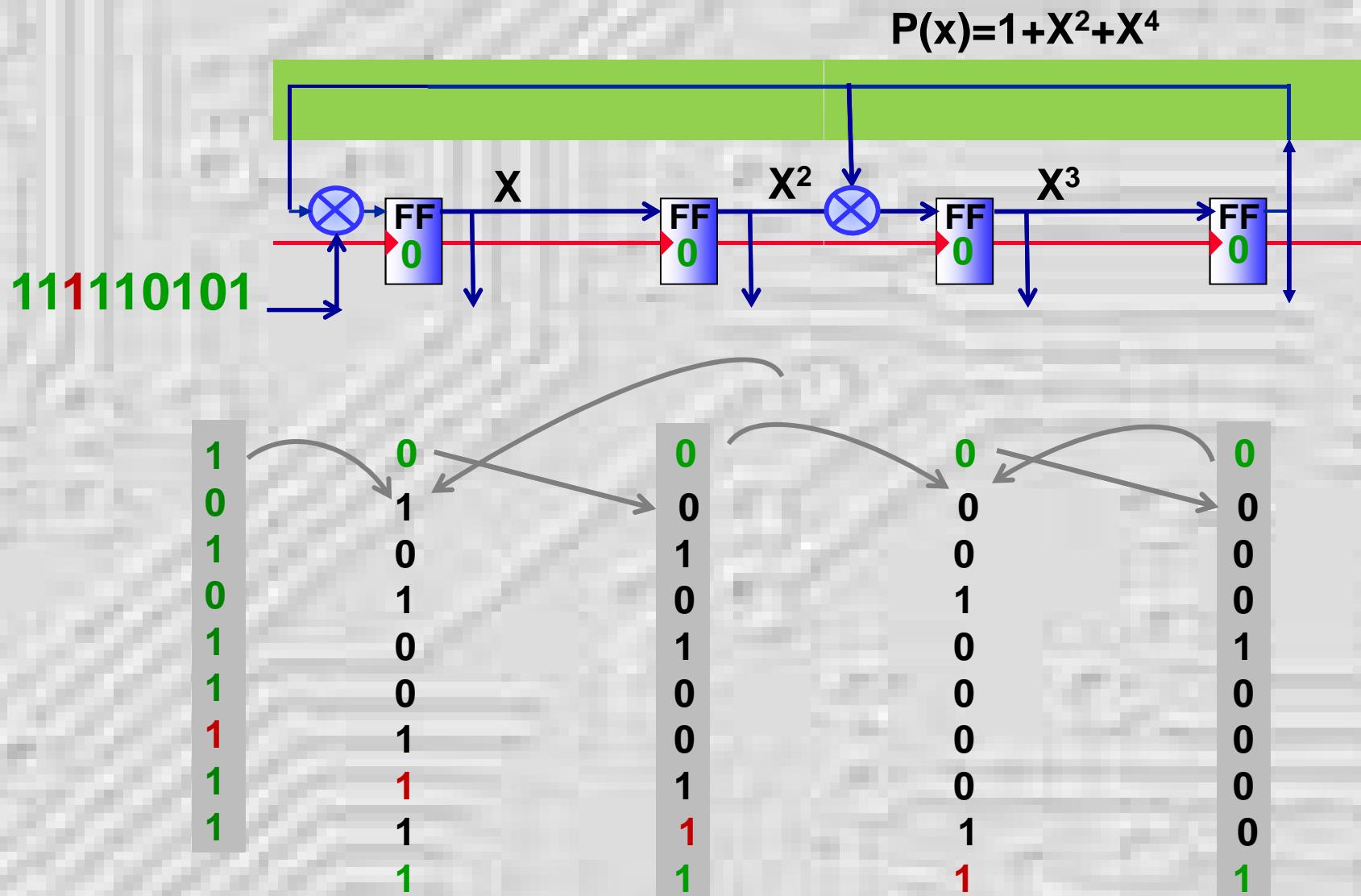
$$P(x) = 1 + X^2 + X^4$$



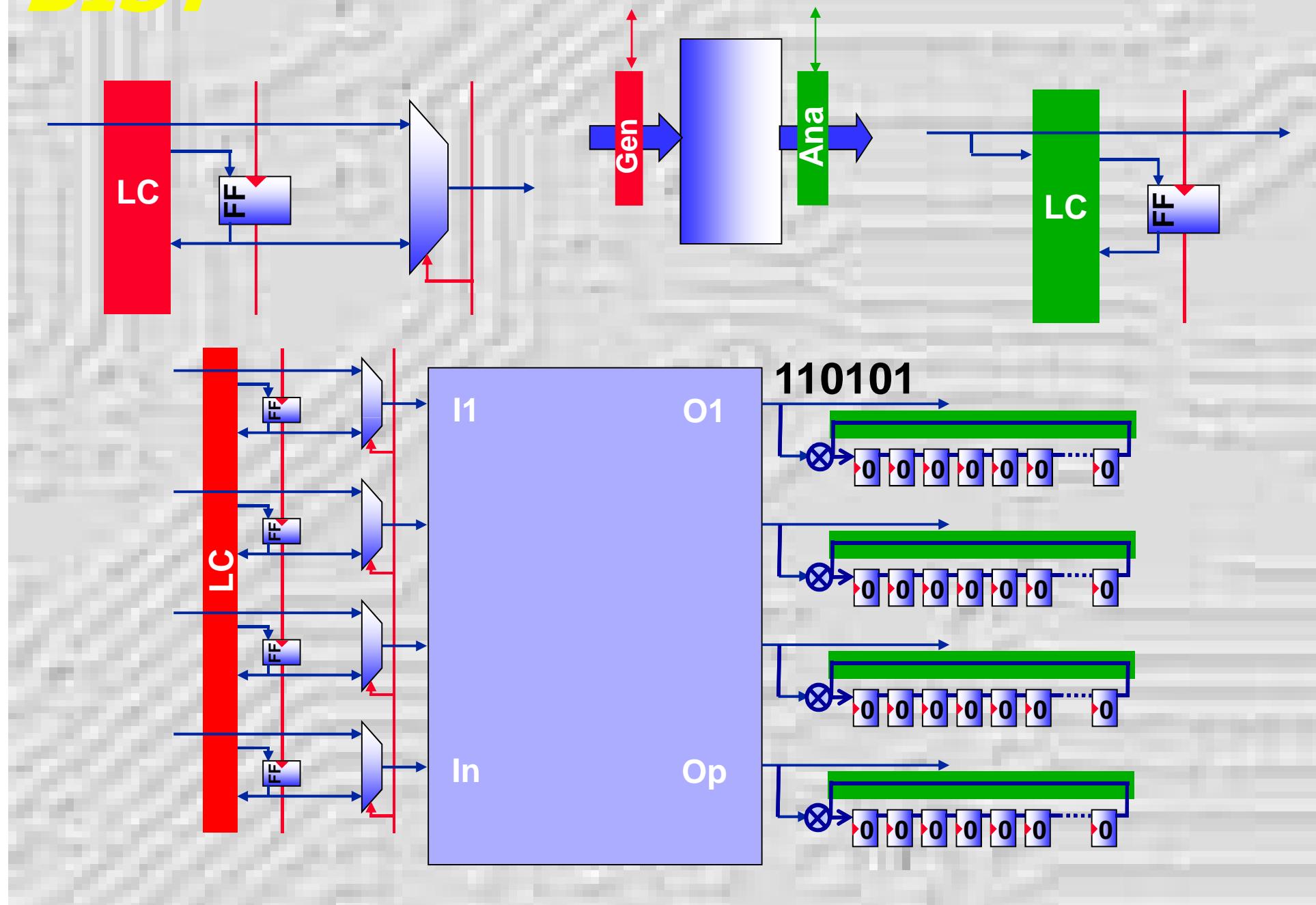
$$P(x) = 1 + X^2 + X^4$$

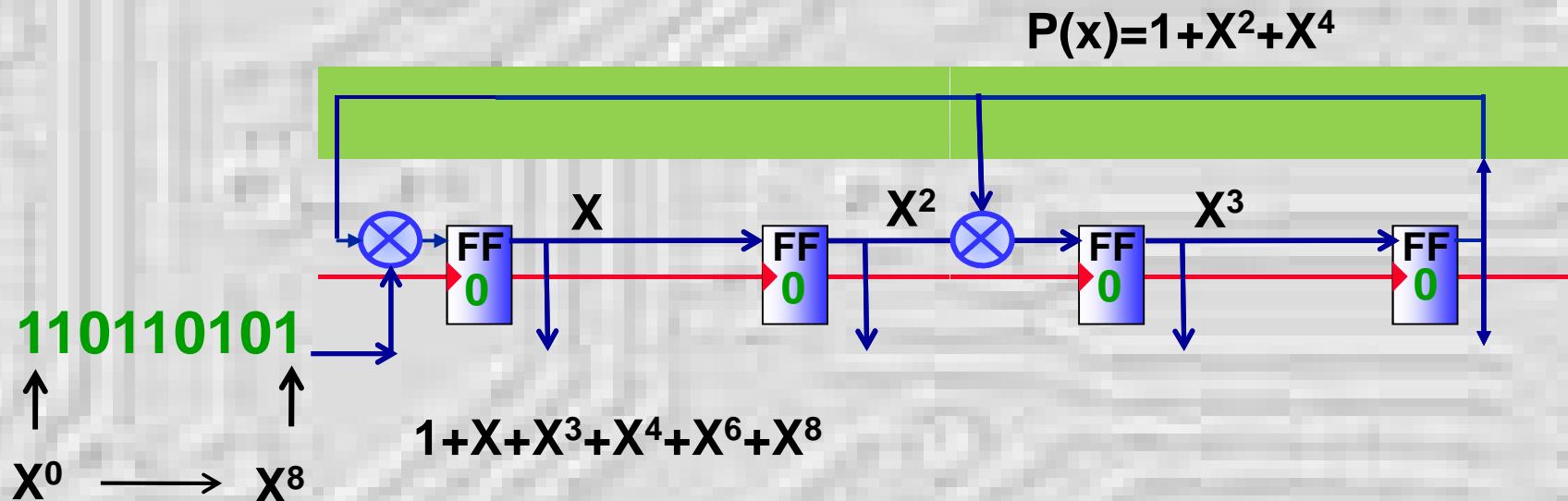






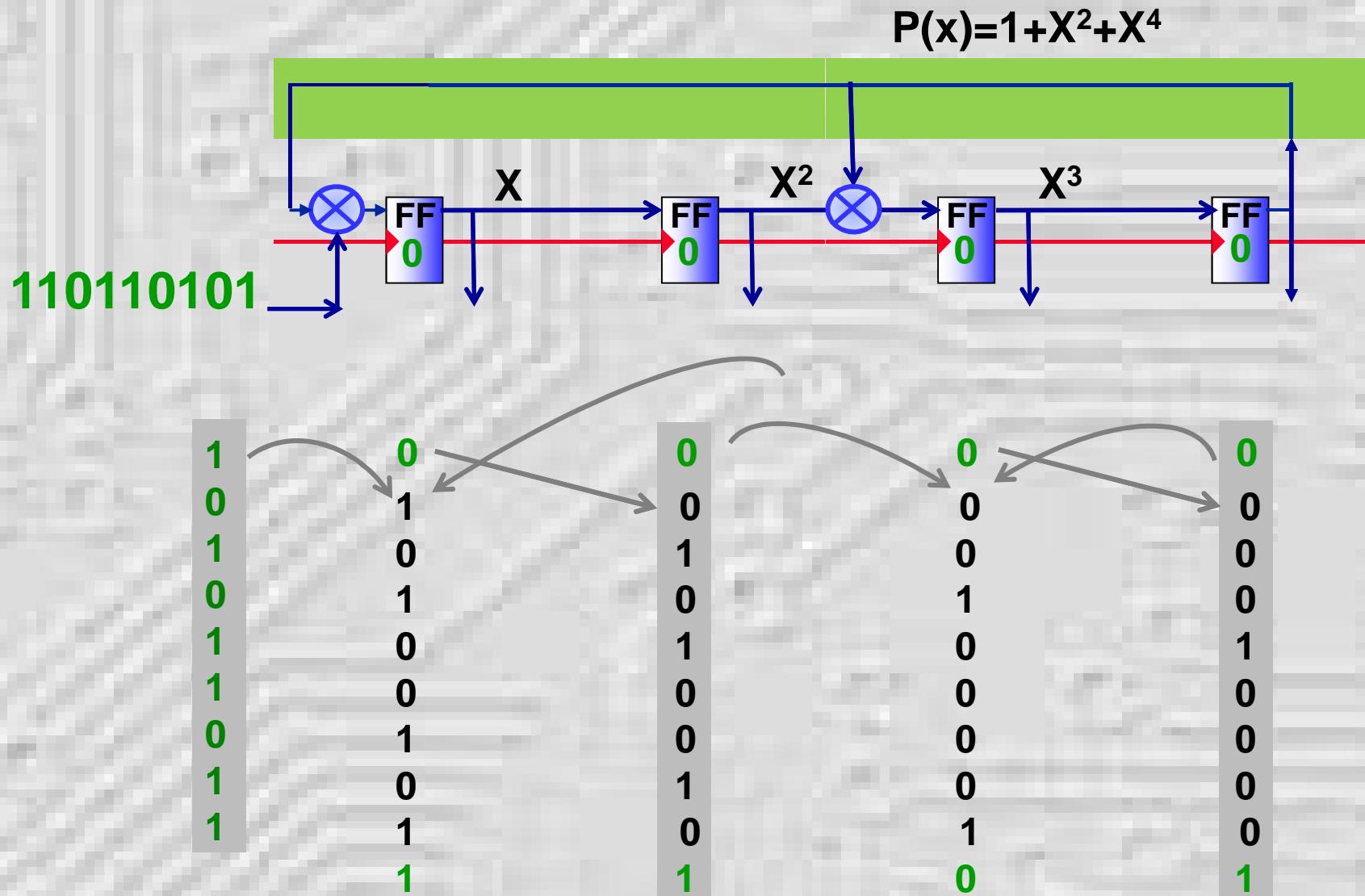
IN2P3

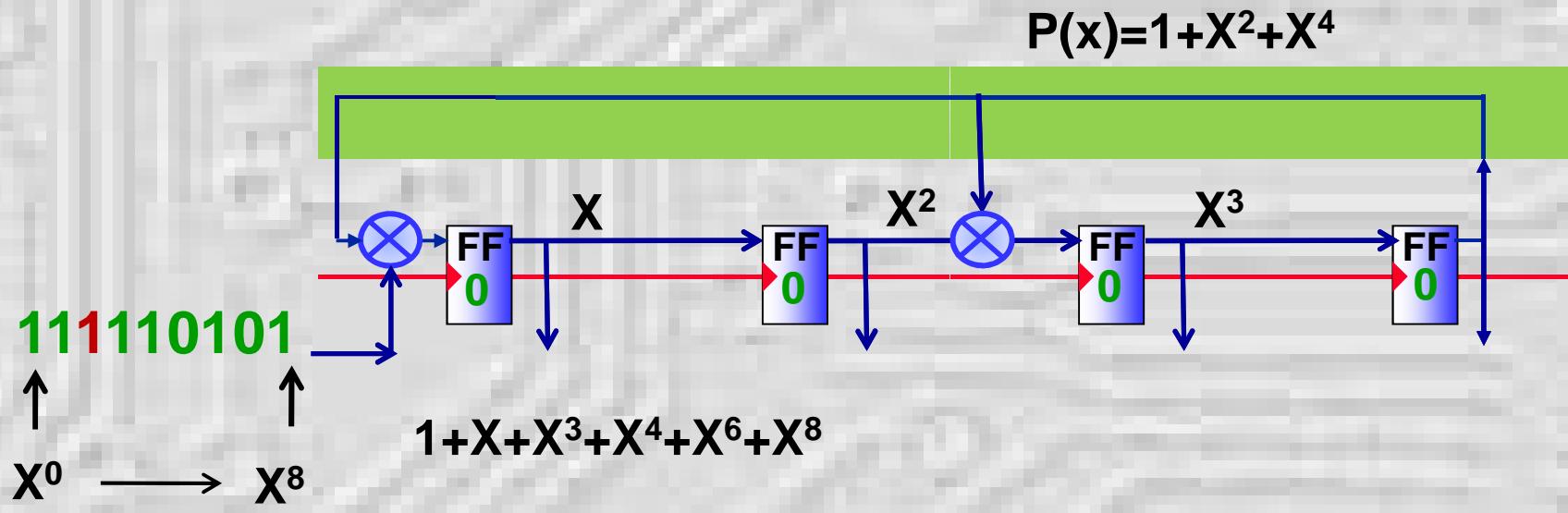




$$\begin{array}{r}
 X^8 + X^6 + X^4 + X^3 + X + 1 \\
 X^8 + X^6 + X^4 \\
 \hline
 0X^8 + 0X^6 + 0X^4 + X^3 \\
 0 \\
 \hline
 X^3 + X \\
 0 \\
 \hline
 X^3 + X + 1
 \end{array}$$

$$\begin{array}{r}
 101011011 \\
 10101 \\
 \hline
 000001 \\
 0 \\
 \hline
 10 \\
 00 \\
 \hline
 101 \\
 000 \\
 \hline
 1011
 \end{array}$$

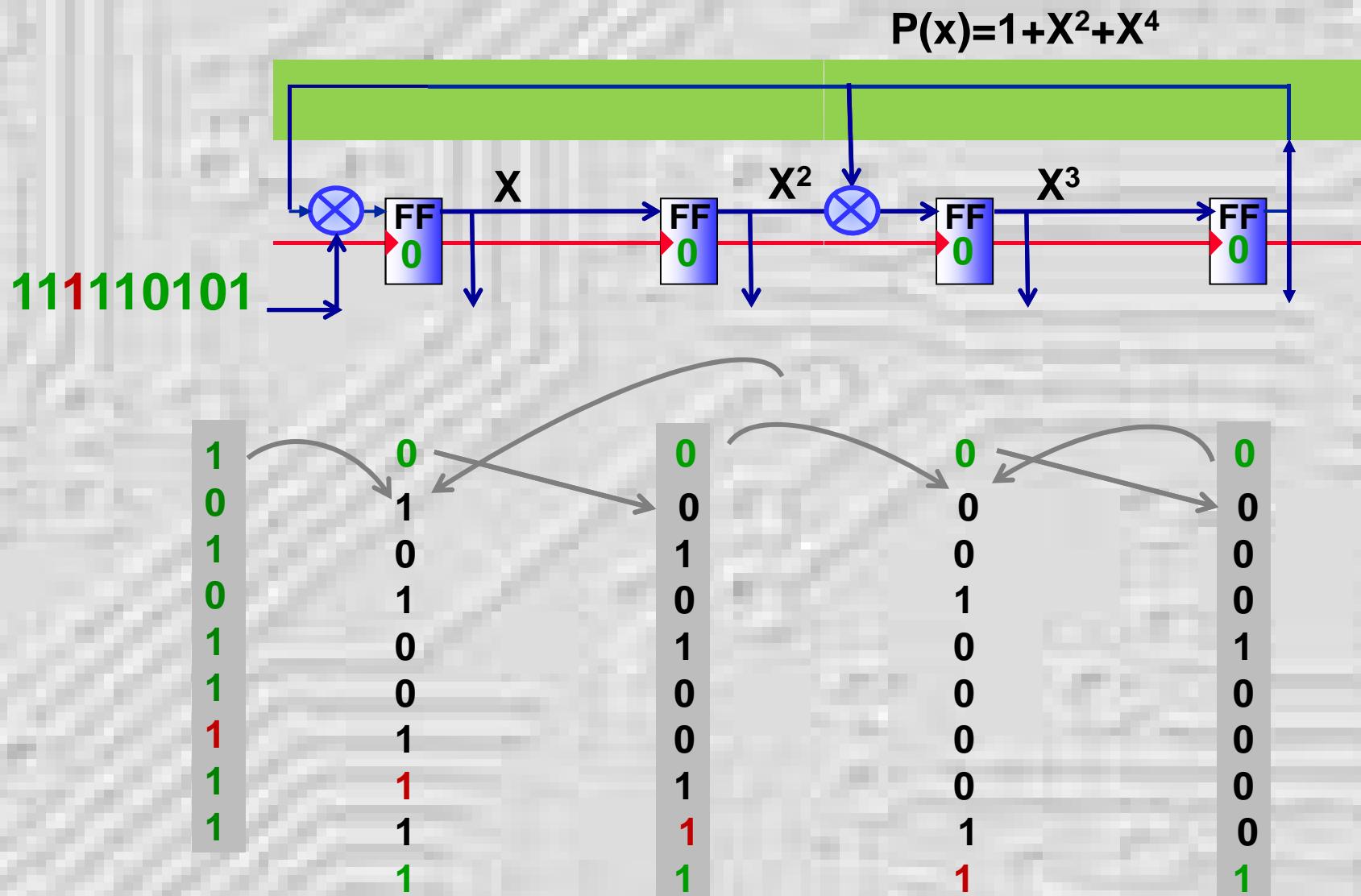


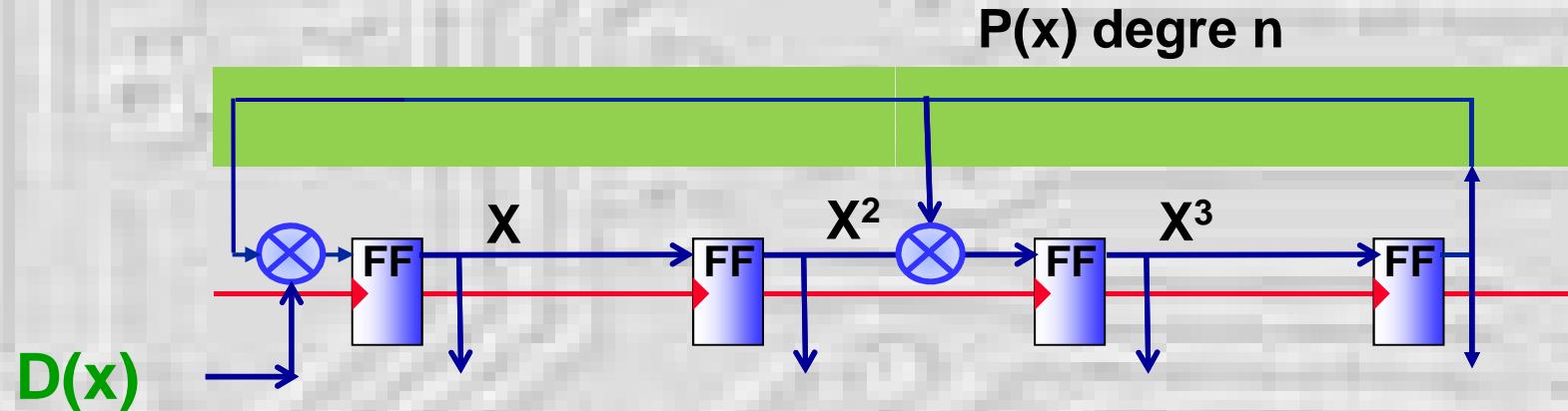


$$\begin{array}{r}
 X^8 + X^6 + X^4 + X^3 + X^2 + X + 1 \\
 X^8 + X^6 + X^4 \\
 \hline
 0X^8 + 0X^6 + 0X^4 + X^3 \\
 0 \\
 \hline
 X^3 + X^2 \\
 0 \\
 \hline
 X^3 + X^2 + X \\
 0 \\
 \hline
 X^3 + X^2 + X + 1
 \end{array}$$

$$\begin{array}{r}
 X^4 + X^2 + 1 \\
 \hline
 X^4
 \end{array}$$

$$\begin{array}{r}
 10101111 \\
 10101 \\
 \hline
 000001 \\
 0 \\
 \hline
 11 \\
 00 \\
 \hline
 111 \\
 000 \\
 \hline
 1111
 \end{array}$$





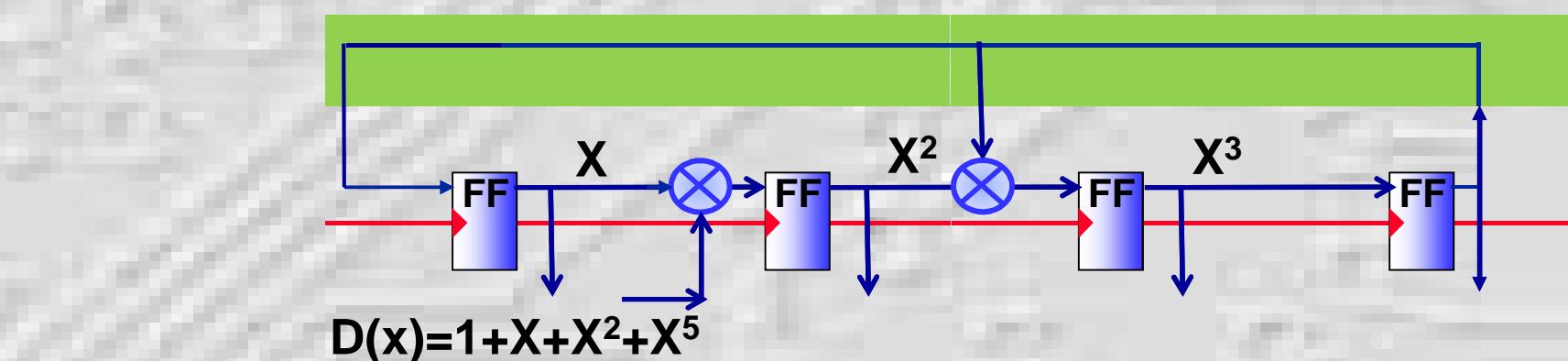
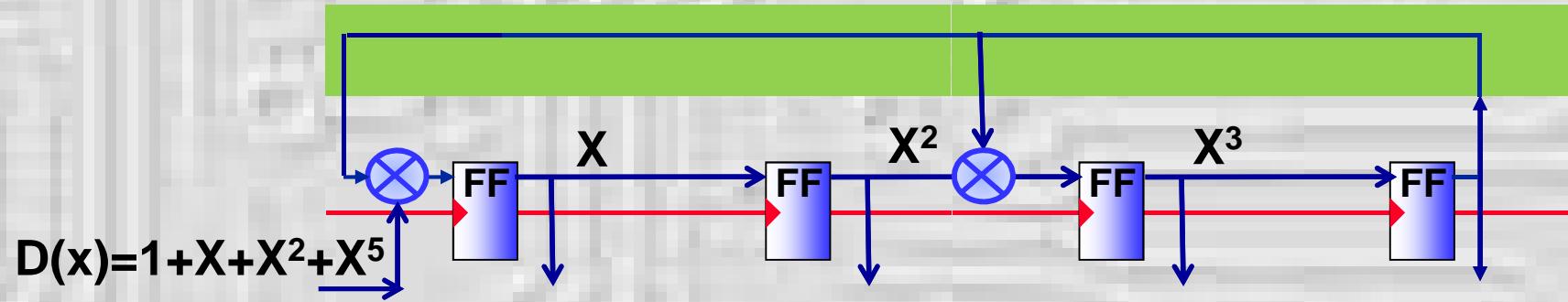
$$D(x) = P(x) \cdot Q(x) + R(x)$$

$$D'(x) = P(x) \cdot Q'(x) + R'(x)$$

Probability $R(x) = R'(x)$

Aliasing

Prob=1/2ⁿ

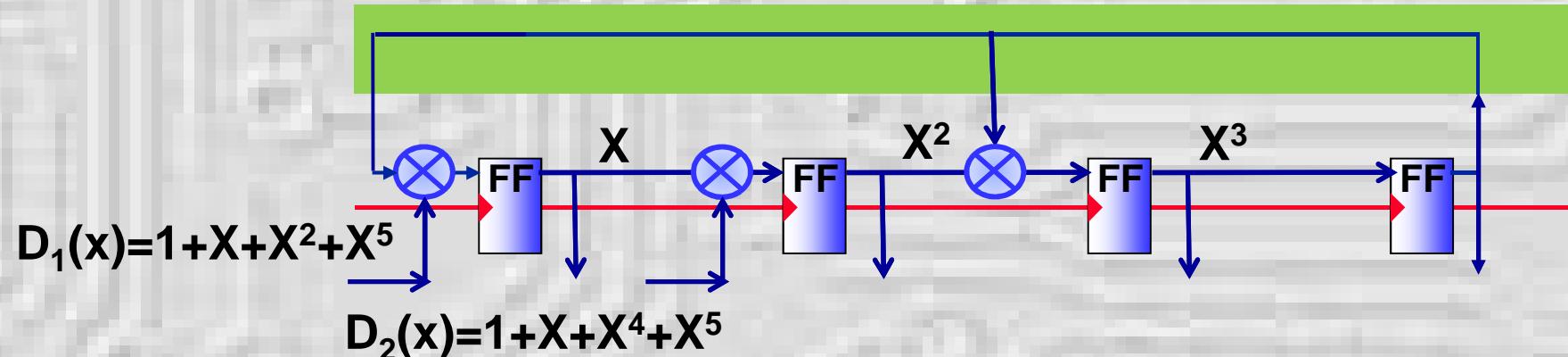


Aliasing

$$P = 1/2^n$$

$$\begin{array}{r}
 X^5 + X^2 + X + 1 \\
 X^5 + X^3 + X \\
 \hline
 1X^3 + 1X^2 + 0X + 1
 \end{array}
 \quad | \quad
 \begin{array}{r}
 X^4 + X^2 + 1 \\
 \hline
 X
 \end{array}$$





$$D_1(x) = P(x) \cdot Q_1(x) + R_1(x)$$

$$D_2(x) = P(x) \cdot Q_2(x) + R_2(x)$$

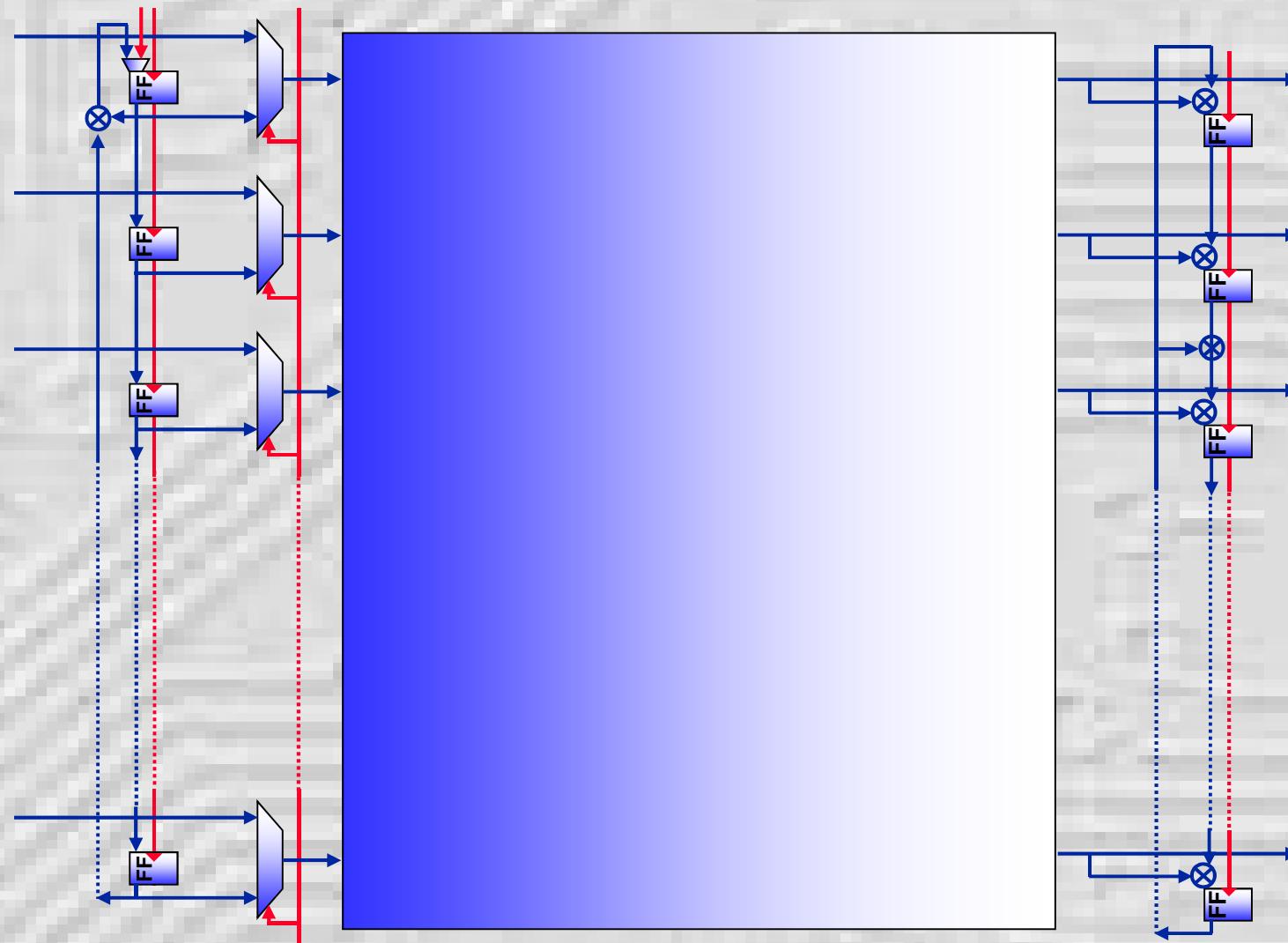
$$\left\{ \begin{array}{l} \rightarrow R(x) = R_1(x) \otimes R_2(x) \\ \rightarrow R'(x) = R'_1(x) \otimes R_2(x) \\ \rightarrow R'(x) = R_1(x) \otimes R'_2(x) \end{array} \right.$$

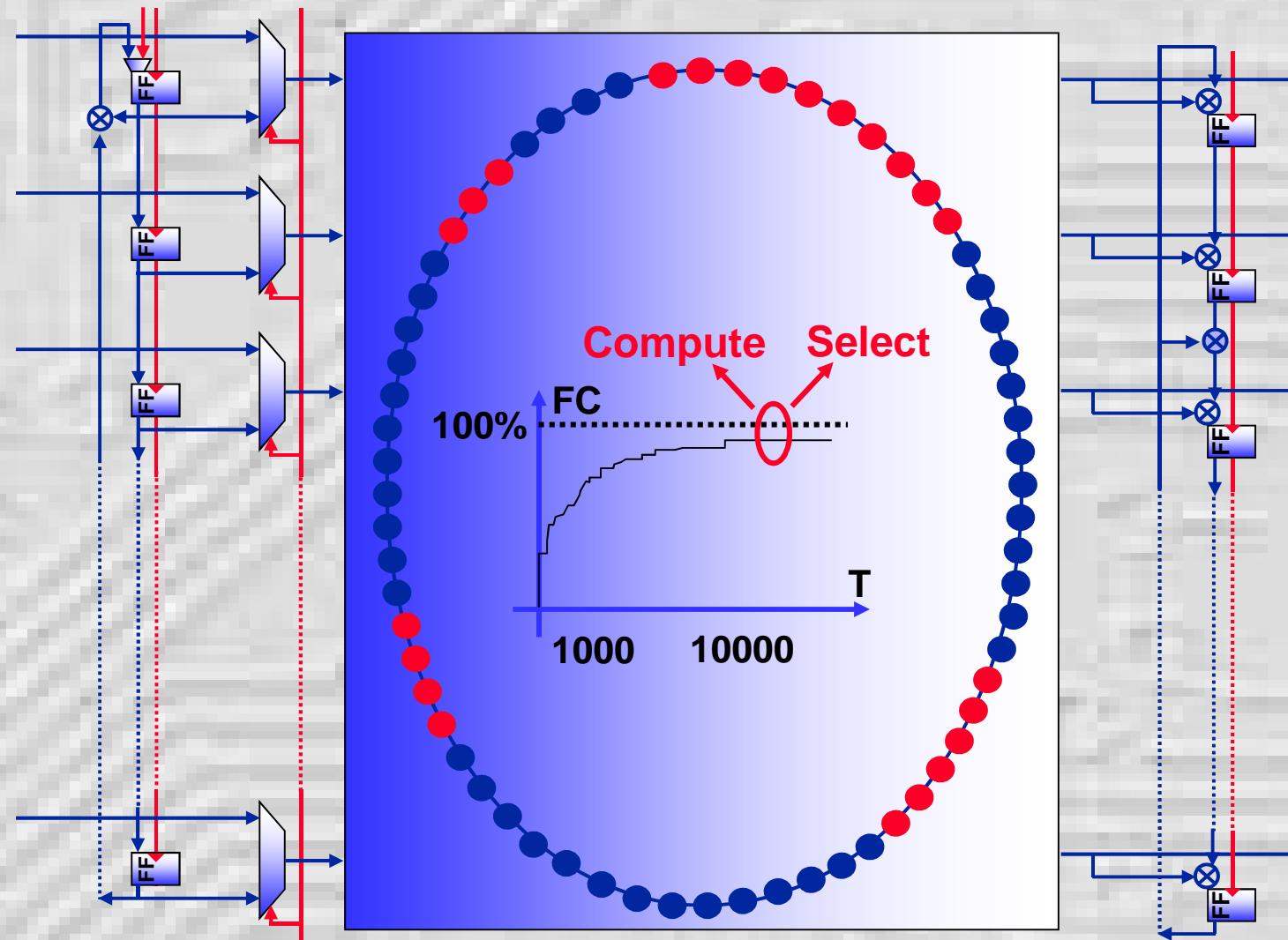
Aliasing

$$P=1/2^n$$

BIST

IN2P3





■ Test Length²

■ Seed/Clock

■ Reconf Polyn

BIST

IN2P3

**IBM
STUMPS**

